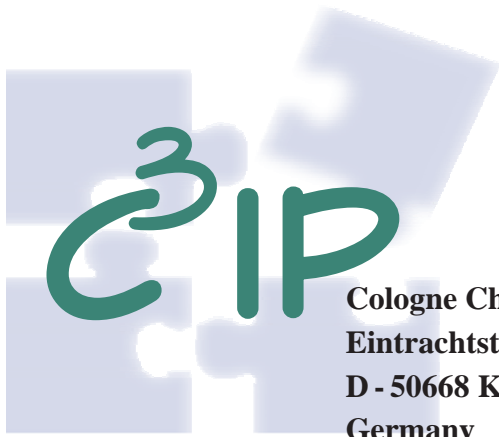


C3 - PLL - 1

**Phase-locked Loop (PLL)
Frequency Multiplier IP Core**

Implemented in DIGICC™ Technology





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1 DIGICC™ technology

Background

Being successful in ASIC design for over ten years, the experience of Cologne Chip's R&D team in digital engineering has led to an in-depth know-how especially in the field of telecommunication interfaces. Millions of sold microchips underline the company's expertise in ASIC and FPGA design. This core competence of Cologne Chip becomes now IP core competence: Cologne Chip introduces several ASIC IPs to the market under the brand name C3IP.



Design approach

The most innovative products of these Cologne Chip IP cores for CMOS devices are based on the entirely new DIGICC™ technology. DIGICC™ increases the range of applications which can be handled by pure digital circuitries.

Up to now PLLs and furthermore analog-to-digital converters (ADC) and digital-to-analog converters (DAC) need a big portion of analog circuitry on the chip. Traditional PLLs need a voltage controlled oscillator (VCO) and loop filter. ADCs – even realized as delta sigma converters – traditionally need some switched capacitor integrators and other analog circuitries. DIGICC™-based cores offer full digital macros for these analog functions. This sounds “impossible” even for the experienced hardware engineer – but it works!

So the biggest benefit of the introduced IP cores is the scalability over a wide range of chip process technologies without requiring design efforts for each new technology. Furthermore, the DIGICC™ IP cores require less silicon space than comparable analog counterparts.

The IP cores can also be integrated in some FPGA technologies at small trade-offs.

All cores are evaluated in silicon and are even used in FPGA technology. They can easily be implemented in different digital CMOS circuits in a broad range of ASIC applications.

The DIGICC™ IP cores are protected by patents and other commercial rights.

Products

Cologne Chip introduces DIGICC™ cores for two fields of applications: C3-PLL and C3-CODEC. For both product families the analog functionality is realized with a completely digital core circuitry.

Please ask our support team for more information on these IP cores.

2 C3-PLL-1 overview

Until today hardware engineers have to rely on analog VCOs for general purpose phase-locked loops (PLL). Cologne Chip has come up now with a fully digital approach: The C3-PLL-1 core for a broad range of PLL applications.

This document describes the PLL IP core C3-PLL-1 including feature list, pinout, block diagram, operational characteristics and electrical parameters.



The C3-PLL-1 is based on the DIGICC™ technology of Cologne Chip, which makes it possible to be easily implemented in all kinds of digital CMOS circuits as a fully digital circuit. Furthermore the lock time is very low while the used circuit area is smaller than that of competing technologies. Because of its pure digital nature, the C3-PLL-1 does neither require any additional PAD or pin nor external or internal loop capacitors. External filters for the supply voltage are normally not needed. A patent is pending for this new Cologne Chip technology.

Technical Features

- Fully digital
- Implementable in any digital CMOS process technology
- Typical oscillator frequency ranges:
 - 0.50 μm : $f_{osc} = 60 \dots 120 \text{ MHz}$
 - 0.35 μm : $f_{osc} = 100 \dots 200 \text{ MHz}$
 - 0.25 μm : $f_{osc} = 140 \dots 280 \text{ MHz}$
 - 0.18 μm : $f_{osc} = 160 \dots 320 \text{ MHz}$
 - 90 nm: $f_{osc} = 200 \dots 400 \text{ MHz}$
- Frequency multiplication by $N = 5 \dots 255$
- Jitter similar to analogue PLLs
- No additional pins or PADs
- No external loop filter or filter capacity needed
- Supply voltage filter is not required
- Very short lock time (worst case 2000 reference clocks)
- FREEZE input to stop oscillator but preserve center frequency (standby mode)
 - very small lock time after FREEZE disable (only some clock cycles)
- FREEZE also reduces power consumption to zero (only leakage current)
- Very small silicon area (< 3000 gates)

Application fields

C3-PLL-1 has some outstanding benefits which makes the IP core interesting for several application fields.

- C3-PLL-1 is a clock multiplier device for CPUs, MCUs and peripheral devices, e.g. USB chips.
- Due to the fully digital approach, C3-PLL-1 can be used in FPGA applications.
- The very short lock time is useful in many applications where the start-up time must be very small (e.g. RF devices), especially for low power applications.

3 C3-PLL-1 pinout

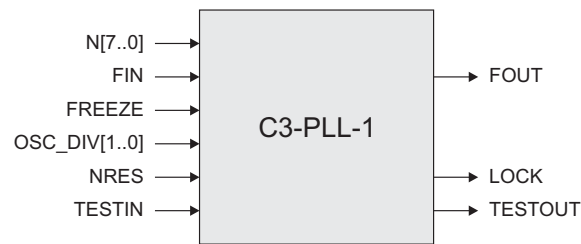


Figure 1: C3-PLL-1 pinout

Table 1: Pin description of C3-PLL-1

Pin name	I/O mode	Description
N[7:0]	I	Frequency multiplication factor $N = 5 \dots 255$
FIN	I	Reference clock with frequency f_{ref}
FREEZE	I	'0' = normal operation '1' = standby mode, oscillator stopped
OSC_DIV[1:0]	I	Oscillator divider factor $M = OSC_DIV + 1$
NRES	I	Low active reset
TESTIN	I	'0' = normal operation '1' = test mode
FOUT	O	Output clock with frequency $f_{PLL} = N \cdot f_{ref}$
LOCK	O	'0' = PLL is unlocked '1' = PLL is locked
TESTOUT	O	Test output

4 PLL operation

The C3-PLL-1 is a clock multiplier PLL which consists of

- a digital controlled oscillator,
- frequency and phase adjustment logic and
- two programmable dividers

like shown in Figure 2.

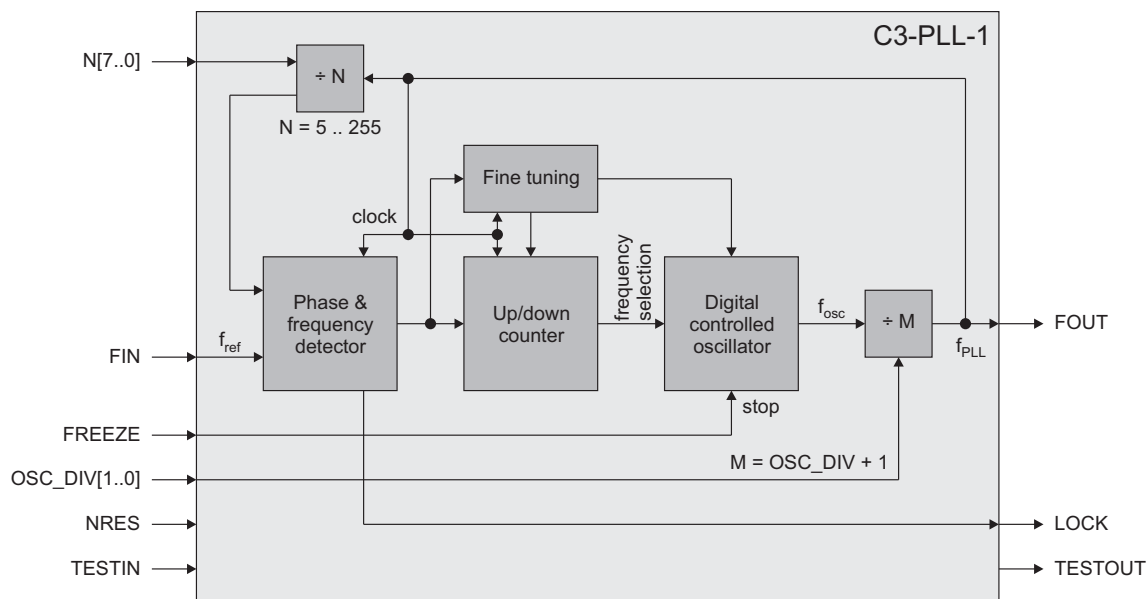


Figure 2: Detailed block diagram of C3-PLL-1

The output frequency

$$f_{PLL} = N \cdot f_{ref}$$

is generated with a digital controlled oscillator. N can be chosen in the range 5 .. 255. The oscillator frequency range depends on the CMOS process technology (listed on page 6) and the delay parameter of the digital library used.

The phase & frequency detector uses only the rising edge of FIN. Thus neither the duty cycle nor the jitter of the falling edge influence the C3-PLL-1 behavior. FIN must be high at least for $1/f_{PLL}$.

The detector output signal triggers an up/down counter which is used to select the frequency of the oscillator. A fine tuning capability is implemented to achieve oscillator frequencies with a high precision.

A new value for N can be set unsynchronized to the reference frequency FIN.

PLL reset

The signal NRES = '0' leads to a C3-PLL-1 reset. Low time should be at least 10 ns. All counters and internal registers are set to an initial value. The PLL starts always with the lowest possible f_{osc} frequency after NRES has been set to '1'.

The output signal FOUT is set to FIN when NRES is statically set to '0'.

Startup phase

During the startup phase, f_{osc} rises without overshoots until the nominal frequency is reached. This procedure takes 2000 clock cycles of f_{ref} at worst case, so that

$$t_{lock} \leq \frac{2000}{f_{ref}} .$$

The LOCK signal is high when the PLL is locked.

Jitter characteristics

Because of the operation method of the PLL, there is some jitter at the output signal FOUT even if the reference signal FIN has no jitter. Additionally there is some jitter induced by supply voltage noise. So if the jitter is a critical parameter special measures should be taken to reduce power supply jitter.

The overall jitter J_{tot} is

$$J_{tot} = J_{det} + J_{pow} + k \cdot J_{in}$$

where J_{det} is the deterministic jitter, J_{pow} is the jitter caused by the power supply and J_{in} is the jitter of the reference frequency f_{ref} . There is a jitter frequency dependent attenuation factor $k < 1$ between the input jitter of f_{ref} and the output jitter J_{in} .

PLL standby mode

The C3-PLL-1 can be switched into standby mode with FREEZE = '1'. Then the oscillator is disabled and the whole PLL logic is unclocked. The power consumption is zero, only process dependent leakage current occurs. The center frequency of the PLL is preserved because the entire state of the digital controller is stored.

After FREEZE has been set back to '0', a small readjustment might be necessary due to temperature drift, supply voltage drift or a slight FIN change. This readjustment takes only a few FIN cycles, typically. So the relock time after FREEZE is significantly shorter than the initial lock time.

The LOCK signal goes low during standby mode.

Selection of output frequency

The oscillator covers a frequency range of

$$\frac{f_{OSC,max}}{f_{OSC,min}} > 2 \quad .$$

The oscillator divider can be used to generate a lower output frequency

$$f_{out} = \frac{f_{osc}}{M}$$

where $M = OSC_DIV + 1 = 1 \dots 4$.

Furthermore, the power consumption of the C3-PLL-1 core is decreased the larger M is chosen. This is due to the fact that main parts of the PLL are clocked by the FOUT pulses.

5 Electrical Performance

The electrical parameters given in Table 2 are valid over the full process range with respect to all process technologies listed on page 6, over the full temperature range 0..70 °C and over the full voltage range $V_{DD} \pm 10\%$.

Table 2: *Electrical performance (over the full process, temperature and voltage range)*

Parameter	Symbol	min.	typ.	max.	Unit
Oscillator Frequency	f_{osc}	100		200	MHz
Multiplication Factor	N	5		255	
Deterministic Jitter ^{*1}			120	250	ps
Jitter from Supply Voltage Noise ^{*2}		1		2.6	ps/mV
Duty cycle of FOUT		40		60	%
NRES low time		10			ns
Power consumption					
in operation			^{*3}		mW
standby ^{*4}		0	10	100	μ W

^{*1}: Clock-to-clock

^{*2}: Clock-to-clock, peak-to-peak noise voltage

^{*3}: Depends on process technology and output frequency

^{*4}: Depends on leakage current of the actual process technology

6 Deliverables

Cologne Chip IP cores consist of a compiled netlist for the destination technology, test vectors for a digital tester environment and behavioral models for evaluation purposes. It can be obtained directly at Cologne Chip. Please contact our Support Team at support@colognechip.com.

The business model for C3IP depends on the specific customer case. It could be for example a general licence for a semiconductor company, a one time licence for an ASIC project or a royalty based model for design houses.

