

## Technical and Commercial Benefits of DIGICC-based C3-PLL

**Reduced Total Cost of Ownership**

1. Traditional analog PLLs meeting all customer requirements might not be available for the desired pure digital target process technology. On the contrary, C3-PLL is a fully digital circuitry based on standard cell libraries only.



**C3-PLL can easily be implemented in all process technologies.**

2. Conventional PLLs in analog technology require at least two pads for so called AGND and AVCC as analog ground and analog supply voltage. Some PLLs even need an additional pad for an external loop filter capacitor. In contrast, C3-PLL requires no pads at all.



**Crucial benefit of C3-PLL, if the die is pad-limited or the package is pin-limited.**

3. Usually external RC filters are required for the analog supply voltage pins AGND and AVCC of conventional PLLs. As a consequence two resistors and two or even four capacitors are needed outside the chip in these classical designs. These components are not needed for C3-PLL.



**No additional cost for external components by using C3-PLL.**

4. C3-PLL disposes of a built-in spread spectrum feature. In many cases competing analog PLLs have such a low jitter that this leads to bigger EMI problems than by using C3-PLL.



**Important advantage for reducing external efforts due to EMI requirements. Especially useful for equipment housed in plastic cases.**

5. Classical analog PLLs for deep submicron (0.25  $\mu\text{m}$  and below) cannot be inserted into the core of the chip. They have to be placed on the pad ring, therefore requiring space in I/O-buffer slots.



**Crucial benefit of C3-PLL, if the die is pad-limited.**

6. Production tests for analog PLLs are „tougher“ and more time consuming than the test of C3-PLL.



**Important fact for reducing test costs.**

7. Analog PLLs are more sensitive to variations of the production process than digital C3-PLL. Lower margins are reducing yield.



**Achieving higher yield of the chip.**

8. In deep submicron (0.25  $\mu\text{m}$  and below) C3-PLL is normally much smaller than conventional analog PLLs.



**The size of C3-PLL scales with chip geometries which means reduced silicon space.**

### Cologne Chip AG

Eintrachtstr. 113 · 50668 Köln  
Germany

Tel.: +49-221-91 24-0

Fax: +49-221-91 24-100

Internet: [www.C3IP.com](http://www.C3IP.com)  
[www.CologneChip.com](http://www.CologneChip.com)  
eMail: [support@CologneChip.com](mailto:support@CologneChip.com)

## Commercial Benefits of DIGICC-based C3-PLL

Additional costs of ownership per chip are in the focus of the following example calculation: DIGICC based C3-PLLs are compared to conventional analog PLLs.

### Sample Scenario

Process technology	0.18µm - 100k logic gates/mm <sup>2</sup>
Silicon size	25 mm <sup>2</sup>
Quantity	200k p.a.
Project duration	5 years

Technical Aspect	Analog PLL	C3-PLL
1. Process technology	- <sup>1)</sup>	-
2. Additional pads	US-\$ 0.08 <sup>2)</sup>	-
3. Additional external components	US-\$ 0.12 <sup>3)</sup>	-
4. EMI requirements	- <sup>4)</sup>	-
5. Additional space in I/O buffer slots	-	-
6. Additional test efforts	US-\$ 0.02	-
7. Higher yield costs	US-\$ 0.01	-
8. Bigger core size	US-\$ 0.03	-
<b>Additional cost in total per chip</b>	<b>US-\$ 0.26</b>	<b>US-\$ 0.00</b>

1) Not applicable in this sample scenario.

2) Required additional silicon space for 2 pads in a pad-limited design:  
 $5\text{mm} \times 0.08\text{mm} = 0.4\text{mm}^2$   
 Cost of additional pads:  
 $0.4\text{mm}^2 \times \text{US-}\$ 0.20/\text{mm}^2 = \text{US-}\$ 0.08$

3) Cost of 2 resistors for AGND and 2 capacitors for AVCC:  
 $4 \times \text{US-}\$ 0.01 = \text{US-}\$ 0.04$   
 Cost of assembly:  $4 \times \text{US-}\$ 0.02 = \text{US-}\$ 0.08$

4) Not quantifiable. Most probably higher costs.



**For a 200k/year project with an overall volume of 1 M pcs., additional cost of ownership totals up to US-\$ 260,000. Even if the legacy PLL is for free!**

