

# **DIGICC™ CODEC Technology**

## **Technology Background**





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# 1 Introduction

## 1.1 Motivation

Analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are widely needed and used in today's semiconductor chips. They convert an analog input signal to proportional digital values, normally represented by a number of bits as a binary number or, in reverse direction, they convert digital values into a proportional analog output signal. Main properties of ADCs and DACs are the numbers of bits commonly named *resolution* and the speed of the device, normally measured in *samples per second*.

One of the most challenging tasks in ADC and DAC design is to adapt the circuitry to ever new CMOS process technology. For digital circuits the number of gates per square millimeter approximately doubles per chip generation. Integration of analog parts in newer deep submicron technologies is much more tough and additionally complicated because the usable voltage ranges decrease with every new integration step. So deep submicron technologies use core voltages below 2 V. Furthermore, some area is needed to realize accurate parameters.

If it were possible to realize an ADC or DAC as a 'pure' digital circuit, no effort would be needed to scale the device for ever new CMOS process technology – and furthermore, the full integration advantage of a digital circuit would be feasible. No special silicon process and test technology known as 'mixed-mode' would be needed as well.

## 1.2 Overview

The goal of the new DIGICC<sup>TM</sup> CODEC technology is that all components in the core of the CODEC are really full digital. The required analog components are moved to the outside of the chip. Only two external resistors and one capacitor are used for the ADC. The DAC uses only one resistor and one capacitor.

The core has one input buffer and one output buffer for the ADC part and one output buffer for the DAC part.

## 1.3 Patents

Several patents were granted in different countries of the world for the DIGICC<sup>TM</sup> CODEC technology. Please contact Cologne Chip for special information or for license requests.

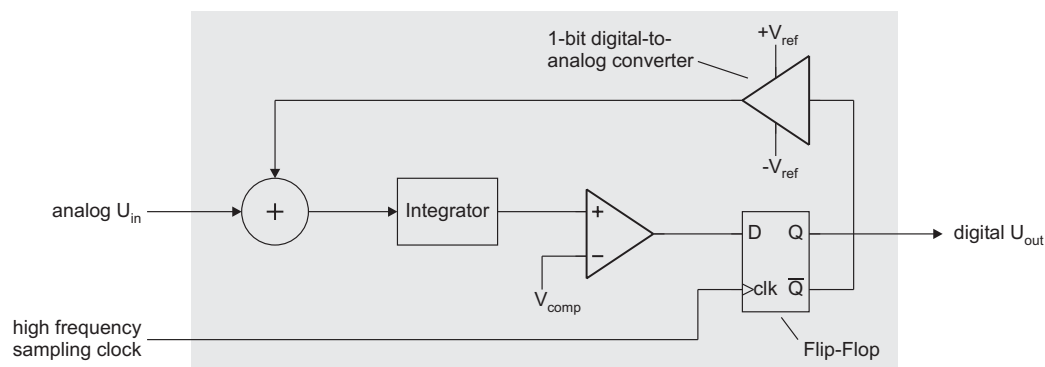
## 2 Pure digital analog-to-digital converter

### 2.1 Overview

One big group of ADCs are delta sigma ADCs which are already known for many years. They implement an oversampling approach which uses an integrator for noise shaping, e.g., and a 1-bit ADC with a much higher sampling frequency of the analog input voltage than the achieved multi-bit output rate. Digital circuitries composed of filters and decimation logic then convert the high speed 1-bit signal into a multi-bit signal with lower frequency. If a 1-bit converter is used, the analog circuitry is very much simplified and many parameters of the chip manufacturing process do not or do only slightly influence the quality of the ADC. Furthermore, a big portion of the ADC circuitry can be realized in pure digital logic which can be reduced in size with every new chip generation.

### 2.2 Simple first order delta sigma ADC

Figure 1 shows a standard delta sigma converter of first order. The most important analog components are the voltage integrator, the reference voltage source and the voltage comparator which in fact is a 1-bit ADC.



**Figure 1:** Standard 1<sup>st</sup> order delta sigma ADC

This structure can be simplified as shown in Figure 2. The integrator is replaced by a simple capacitor, the voltage adder is replaced by two resistors, the comparator is replaced by an input buffer of a pure digital chip and finally, the voltage reference is replaced by the supply voltage of the chip.

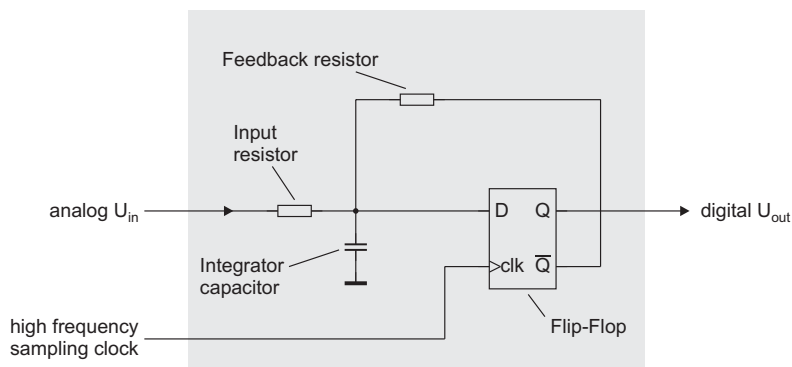
This approach is already known for several years, but the performance is poor. A resolution of approximately 7 bit can be reached, what is enough for simple low resolution ADCs. The benefit of the structure is that it is easy to use a high oversampling frequency because there is no switched capacitor integrator.

### 2.3 Improvements to achieve high resolution

#### 2.3.1 Problems

The RC integrator which replaces the integrator has many advantages compared to a traditional switched capacitor approach with amplifier. For higher performance the integrator must meet special requirements – mainly speed and accuracy. Furthermore, the integrator needs some chip area and





**Figure 2:** *Simplified 1<sup>st</sup> order delta sigma ADC*

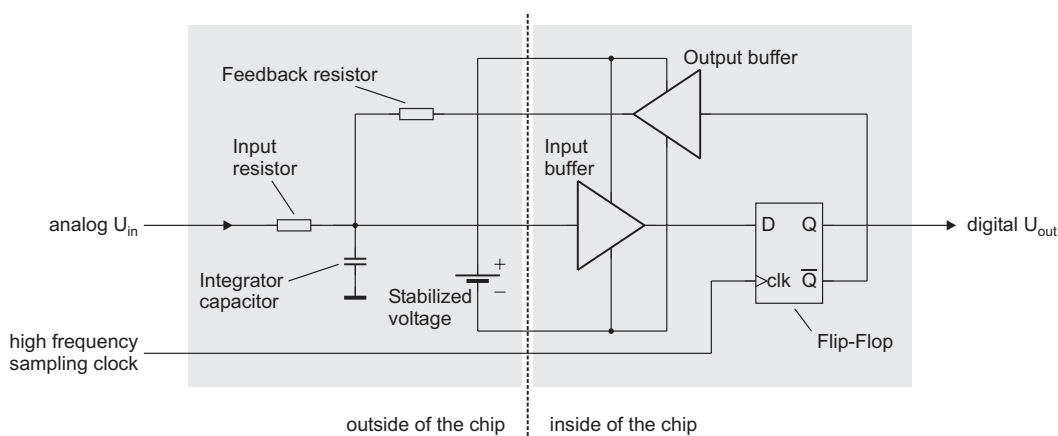
additional operating power for the amplifier.

In contrast to this, the RC integrator has nearly no parasitic disadvantages. It does not consume any additional operating power. The accuracy is only limited by the very small noise level of the resistor and the capacitor. An absolute accuracy of better than 1% is of very low cost for external components. However, in voice or xDSL applications the absolute accuracy of the ADC is even not a key feature. Much more important is the resolution and linearity.

The exact time constant of the RC element is not critical if the voltage swing on the capacitor is kept small. The input voltage range can be much higher than the supply voltage of the digital chip because of the attenuation which is caused by the input resistor. The up to now known poor quality of this ADC can be overcome by improving two things:

- accuracy of the comparator threshold voltage
- accuracy of the feedback output voltage

These improvements are explained in the following sections.



**Figure 3:** *1<sup>st</sup> order delta sigma ADC with DIGICC™ technology*

### 2.3.2 Accuracy of the comparator threshold voltage

The accuracy of the input threshold voltage of the comparator which is now replaced by a simple input buffer is mainly influenced by the noise on the buffer supply voltage. This is due to the fact that the threshold voltage for a normal input buffer is a share of the supply voltage. The noise can easily be reduced if the supply voltage connections of the buffer are routed to special power pads to feed the buffer with a special low noise voltage or a noise reduction for the buffer is implemented on chip. Furthermore, a normal CMOS type digital input buffer should be modified so that the supply current is reduced. Because the buffer is operated at the digital switching level (normally  $0.5V_{DD}$ ), a normal digital buffer would draw a big current from the supply. By using smaller transistors the current can be reduced dramatically only leading to a reasonable increase in the delay characteristics of the buffer. As shown below, the delay time is normally not a critical value, sometimes a bigger delay in the feedback path is even wanted. In some cases it is an option not to use a special input buffer. Instead only the ESD protection circuitry is preserved and an inverter of the chip core is used. Core transistors normally are small enough that the supply current even at the switching point is very low.

Most important is that even the accuracy of the ‘comparator’ is not a key feature for first order delta sigma ADCs. It is even recommended to add a noise source with well known characteristics to the comparator level to avoid long cyclic patterns in the digital output.

### 2.3.3 Accuracy of the feedback output voltage

Unfortunately, noise and inaccuracy of the reference voltage directly influence the performance of the ADC. So if the supply voltage instead of a specially stabilized reference voltage source is used, the performance of the ADC is decreased. Here the output buffer of the digital chip is responsible for the connection to the supply voltage. By using additional power pads for this output buffer which are feed by a noise reduced stabilized voltage or an internally on chip stabilized voltage the performance of the ADC can be increased.

In many cases even a good blocked and decoupled supply voltage is already sufficient. Noise portions which come from the sampling clock or even multiples of it are not influencing the performance of the ADC. This is due to the fact that all integer multiples of the clock frequency influence each output pulse of the ADC in the same way. So the effect is the same as an output voltage with a small offset. For voice CODECs also very low frequencies and the exact scaling of the ADC are no key aspects.

## 2.4 Reducing of the output frequency

Because the resolution increase compared with the oversampling ratio for a first order delta sigma ADC is only 9 dB/octave, the oversampling ratio for a 78 dB voice codec ADC should be at least 9 octaves which means a sample clock frequency ratio of 512 : 1. For a sample clock of 8 kHz this means a high sampling clock for the converter of 4 MHz. This can easily be achieved. To reduce effects of EMI and reduce the power consumption of the ADC it is useful to implement some methods to reduce the maximum feedback frequency going out of the output buffer. This does not significantly reduce the resolution of the ADC because the feedback pulses are limited in frequency but the time resolution of the pulses is preserved. The reduction of the output frequency can be done by additional digital logic in the feedback path.



## **2.5 RC network**

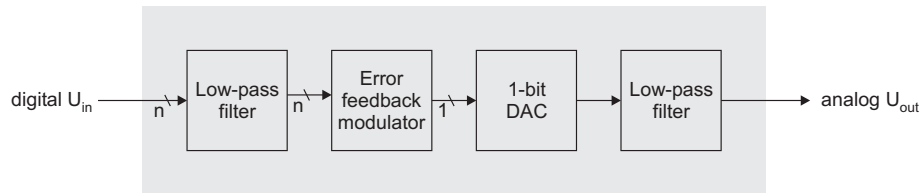
The best way to improve the noise shaping is to increase the external RC constant. This is limited because a too big time constant of the RC in the feedback path only generates a small voltage swing on the capacitor and leads to a very noise sensitive input.

## **2.6 Filter and decimator**

Using small voltage swings on the capacitor (e.g. approx. 20 mV for a 3.3 V LVCMOS type input buffer) result in an integrator characteristic which is nearly identical to a real integrator. So for the above mentioned 78 dB ADC no special precautions or changes must be made to the decimator and filters compared to a traditional delta sigma ADC. This preserves the ability to use well known filter / decimator circuitries as used for traditional delta sigma ADCs.

### 3 Pure digital digital-to-analog converter

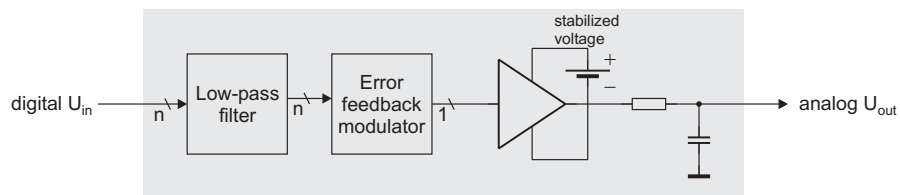
The digital-to-analog (DAC) converter can also be implemented in pure digital technique. Figure 4 shows a typical DAC design approach which is well-known from literature.



**Figure 4:** *Standard delta sigma DAC*

An error feedback modulator converts the multi-bit signal in a 1-bit data stream with an high symbol rate. An output buffer converts this 1-bit digital signal into an analog signal which is applied to a simple RC filter.

Figure 5 gives a detailed view to the analog part of the DAC. The quality of the output voltage is mainly influenced by the stability of the buffer's power supply. This can be improved by using separated power pads for the output buffer and by feeding the buffer with a special noise reduced voltage.



**Figure 5:** *DIGICC delta sigma DAC*

## 4 Example applications

### 4.1 Implementation as voice CODEC C3-CODEC-G712-4

#### 4.1.1 Overview

The herein described DIGICC CODEC technology is used in a CODEC IP core with four separate CODECs compliant to the telecommunication standard ITU-T G.712 [1]. So a simple pure digital chip or even a FPGA can be used as a voice CODEC. For FPGAs in most cases additional external buffers must be used because the normal buffers cannot be feed by special voltages and a nearly zero hysteresis for the input buffer is recommended.

#### 4.1.2 Measurement results

For the first implemented G.712 PCM voice CODEC extensive measurements were made. Figure 6 shows the signal-to-noise measurement results of an FPGA implementation with external buffers in the input and in the output path. These were separately supplied to reduce noise and other interferences.

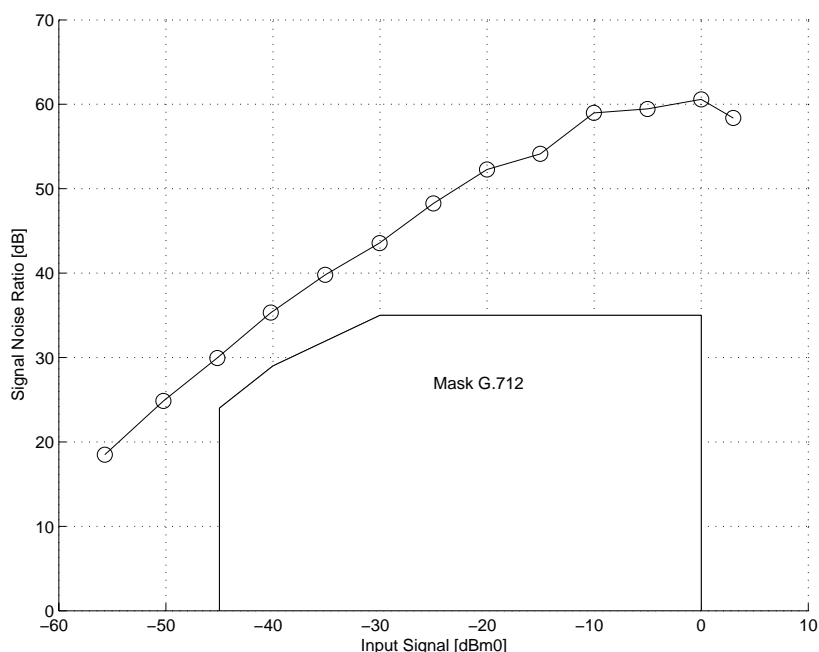


Figure 6: SNR as function of input level

The mask in Figure 6 is according to Figure 12 in ITU-T G.712 [1] as a requirement from analog E4in to digital Tout. The signal representation in Figure 6 is linear, i.e. it is not a-law or  $\mu$ -law coded. The -40 dBm0 input level means an input signal of 43 dB below full range. Figure 6 shows a signal-to-noise ratio (SNR) of 35 dB in this case. This results in an effective resolution of 78 dB at -40 dBm0 input level.

## **4.2 Applications for higher input frequencies**

For modern xDSL systems, ADC with higher sampling frequencies are needed. The shown ADC can be improved in several ways. First, we can replace the first order delta sigma converter by a second order converter. This also can be realized with three additional passive external components. Because then there is a bigger difference to a front-end with two real integrators the digital signal processing stage must be modified to reflect the different external circuitry.

Also for many applications we can use a very high sample frequency and a multiple flip-flop (FF) sample stage. The sample frequency can be easily increased into the 1 GHz range with nowadays 0.13  $\mu\text{m}$  chip technology. With multiple FF stages each using a different phase of the clock frequency the virtual and usable sample frequency is increased into the 10 GHz range. Because of the means to reduce the output frequency of the output buffer described in section 2.4 we can exploit the high sample frequency even using reasonable feedback frequencies. This leads to feedback pulses of high time resolution because of the high internal sampling frequency. This is similar to a delta sigma ADC with a multi-bit feedback path. So the performance of a multi-bit delta sigma converter is achievable with a 1-bit feedback approach which is much simpler and more cost effective.

## 5 Conclusion

DIGICC™ is a high sophisticated new approach for high performance delta sigma type ADCs and DACs. It realizes mixed mode requirements with pure digital IP cores and few external low cost components.

The technology is usable for a big range of ADCs and DACs from slow PCM voice CODECs to higher speed xDSL applications. One of the most important aspect is that the converter can be implemented on a pure digital chip and so it can be entirely described with HDLs like, e.g., VHDL or Verilog. So a seamless integration in every new chip process technology is achieved and the scaling factor of a new digital chip generation can be fully exploited.

## References

- [1] The International Telegraph and Telephone Consultative Committee (CCITT), International Telecommunication Union (ITU). *CCITT G.712: General Aspects of Digital Transmission Systems; Terminal Equipments. Transmission Performance Characteristics of Pulse Code Modulation...*, 1992.



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