



HFC-SP

SA3

5V and 3V3 operation

SIEMENS K1403 Measurement Protocol

Name of company:	TRPS
Test sequence name:	B2x-LP
Name of operator:	K.Jauernik
Organisation unit:	Cologne Chip
Device version number:	SIEMENS,7KK1403,102011112020112010.30412 533**2525**4141
Test object name:	HFC-SP SA3
Test object description:	SIEMENS,7KK1403,102011112020112010.30412 533**2525**4141

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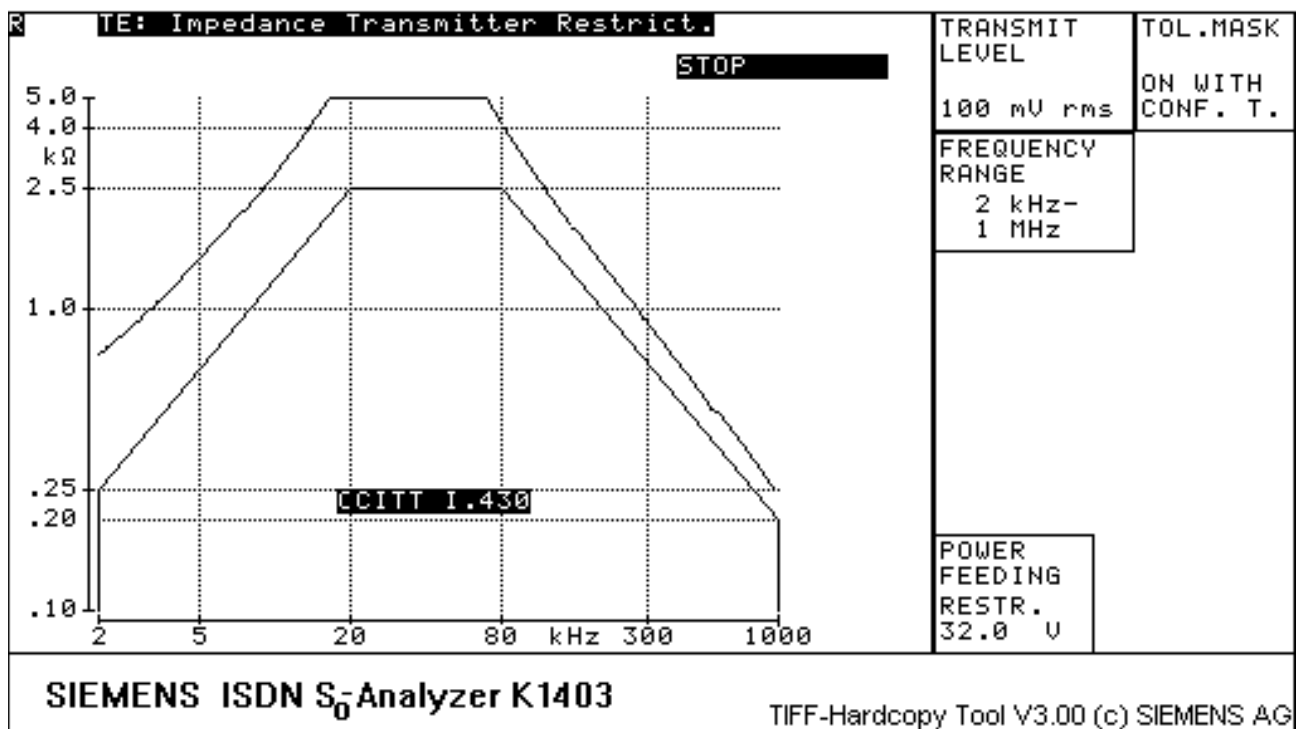
SA3 with HFC-SP 5V operation

Impedance Transmitter

1. V30-12.4

Test A: output impedance when transmitting a binary one in state F3, restricted power at 32V

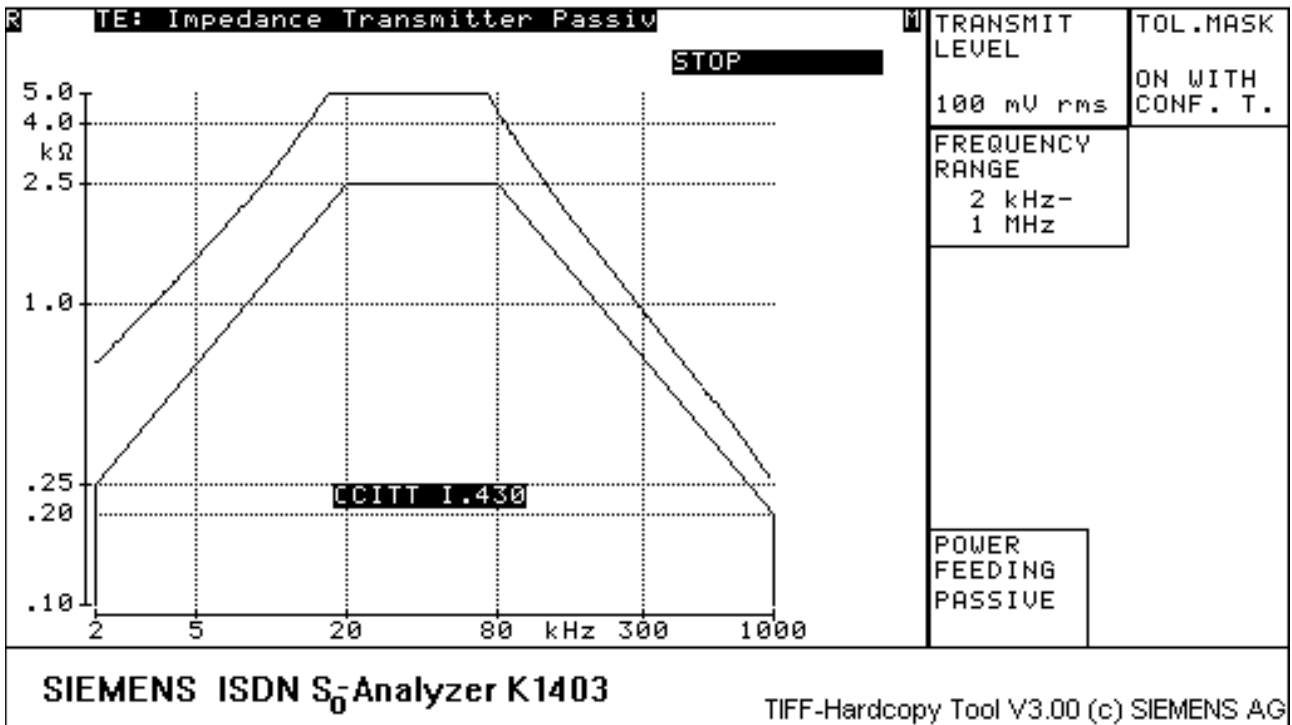
Conformance PASSED



29. V30-12.25

Test D: output impedance when transmitting a binary one in state F1

Conformance PASSED



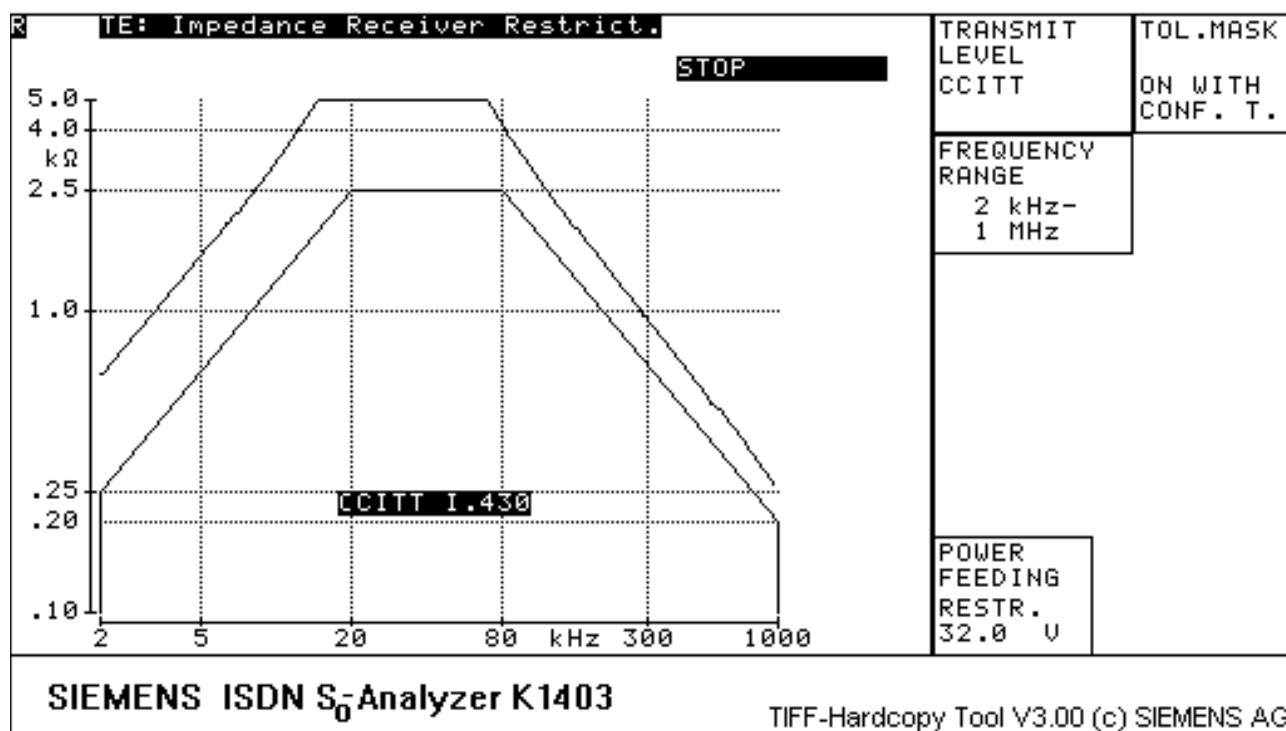
HardCopy #10

Impedance Receiver

24. V30-16.4

Test A: Receiver input impedance in state F3, restricted power at 32V

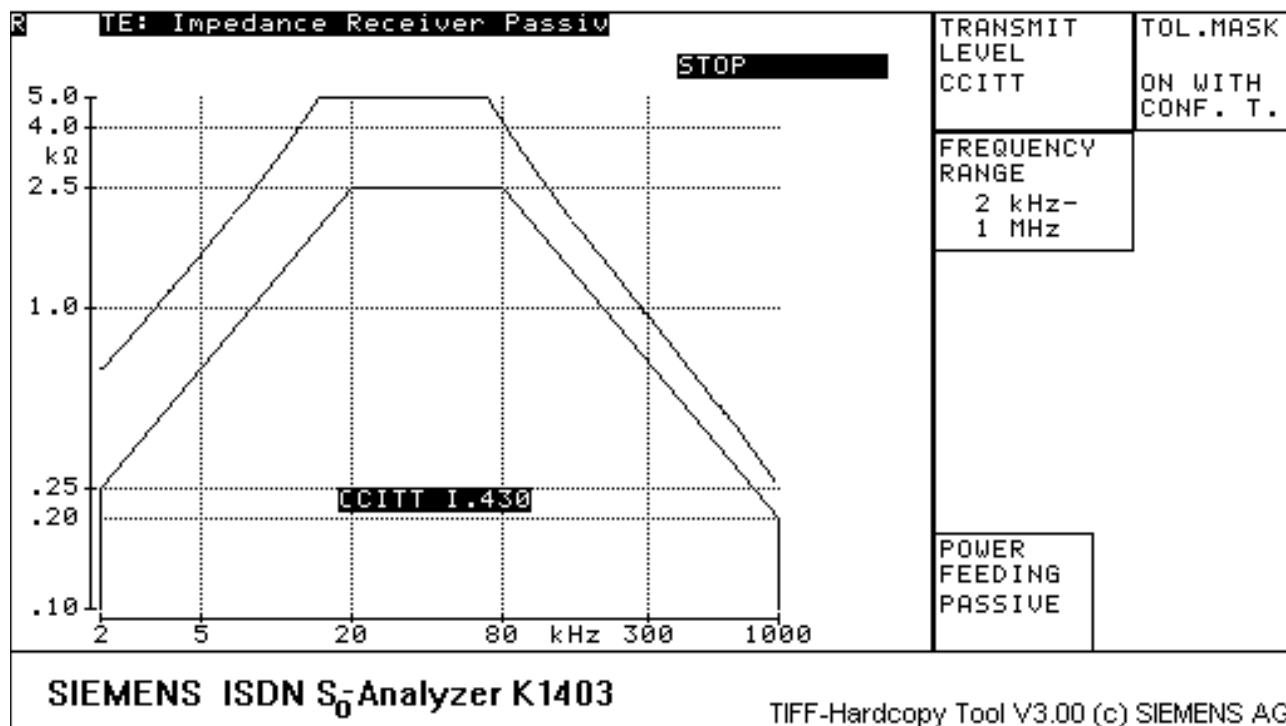
Conformance PASSED



31. V30-16.9

Test C: Receiver input impedance in state F1

Conformance PASSED

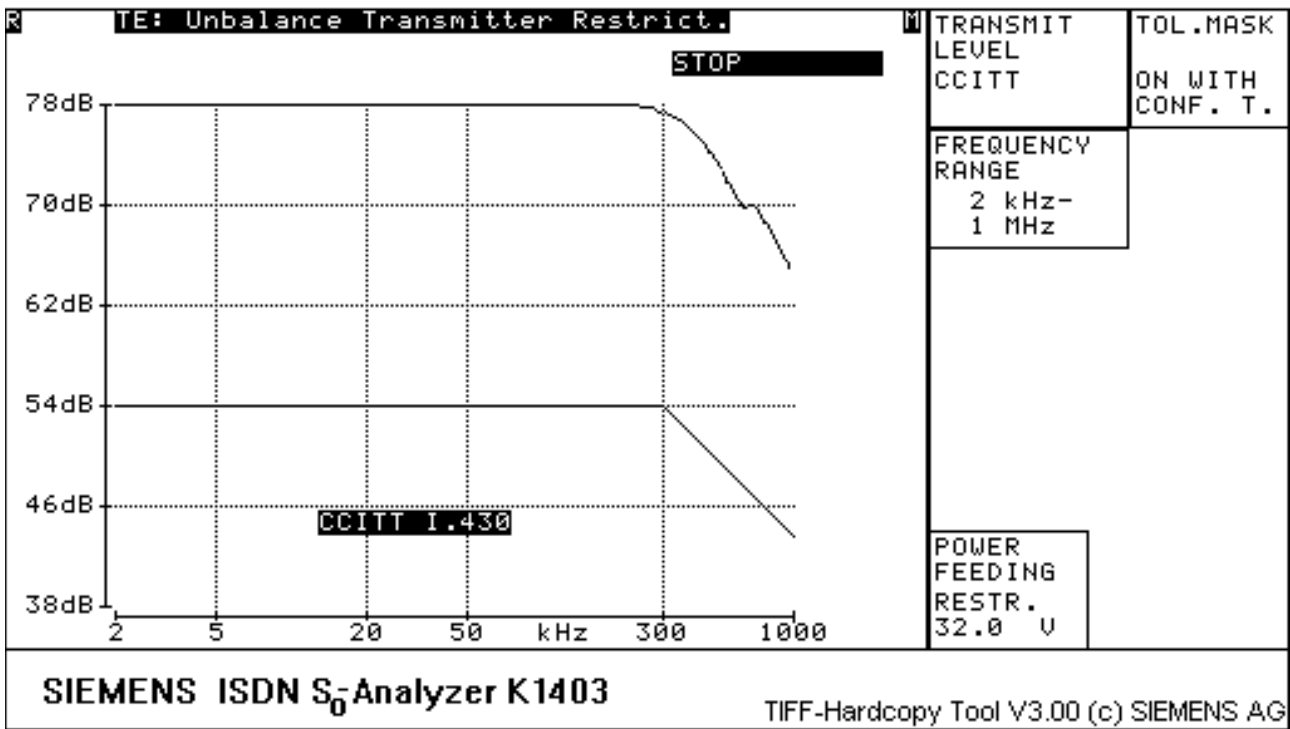


Transmitter output longitudinal conversion loss

22. V30-15.4

Transmitter output longitudinal conversion loss in state F3, restricted power at 32V

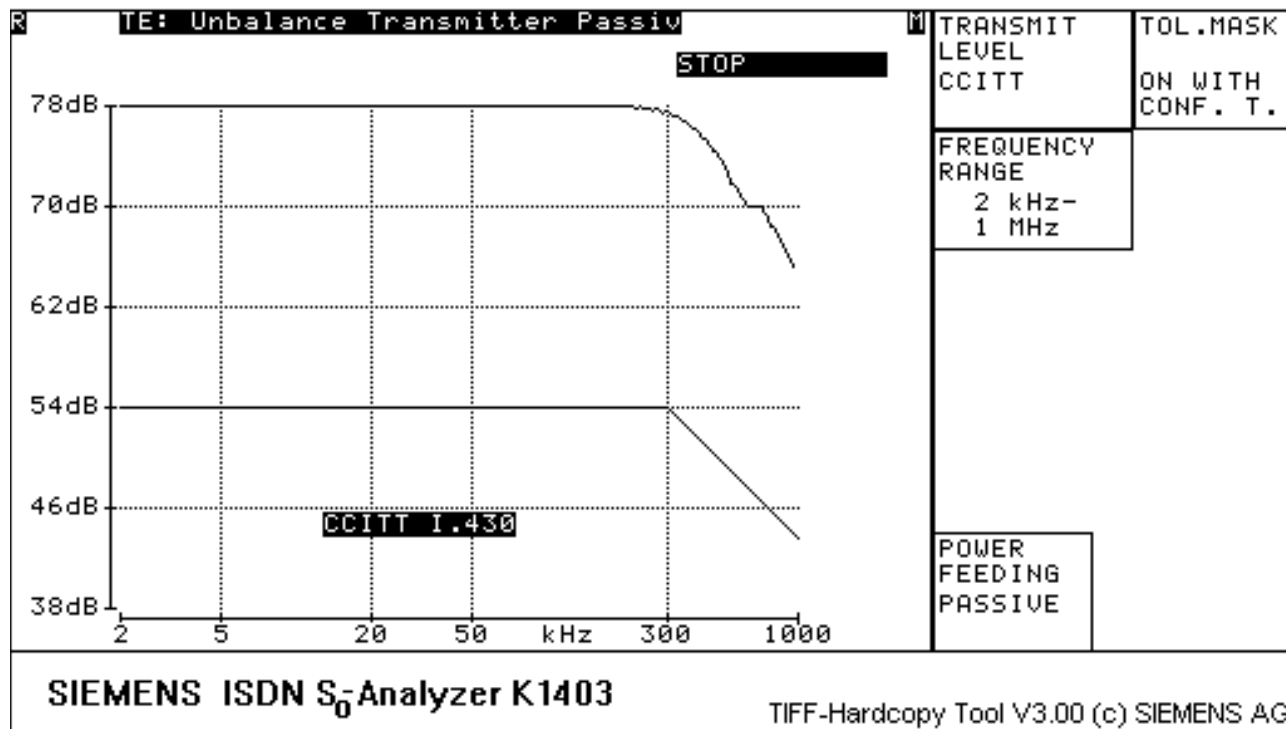
Conformance PASSED



30. V30-15.5

Transmitter output longitudinal conversion loss in state F1

Conformance PASSED

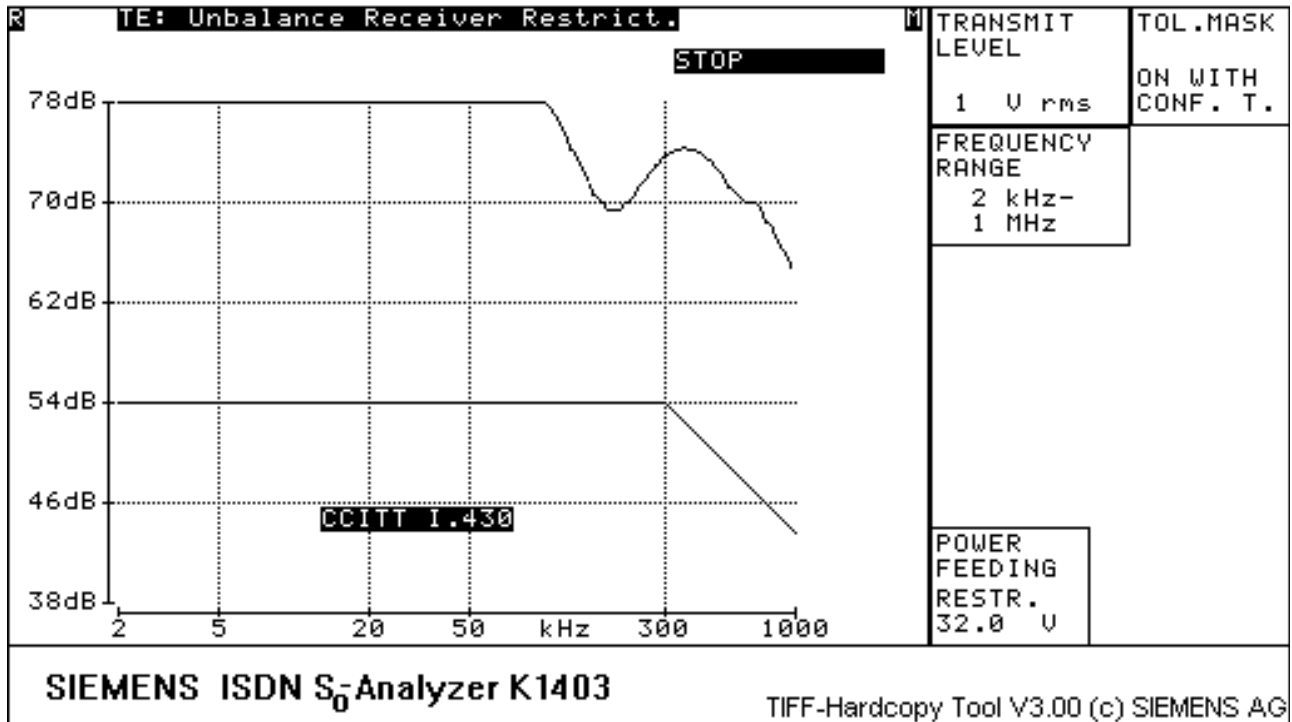


Receiver unbalance about earth

28. V30-18.4U

Receiver unbalance about earth (longitudinal conversion loss) in state F3, restricted power at 32V

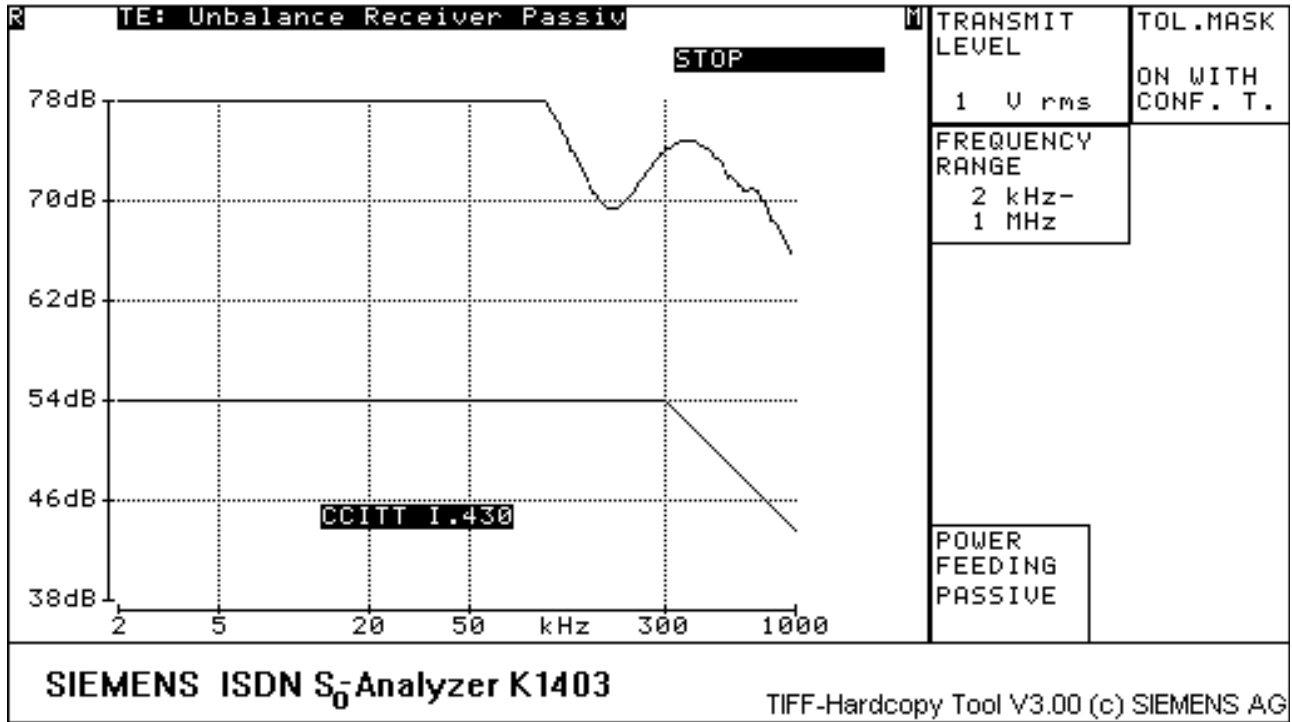
Conformance PASSED



32. V30-18.5U

Receiver unbalance about earth (longitudinal conversion loss) in state F1

Conformance PASSED



output impedance

2. V30-12.8

Test B: output impedance when transmitting a binary zero, positive pulses into a 50R load, restricted power at 32V

double pulses into 50R (R+,R-,R+-)
isolated pulses (R+) w. loop

Conformance PASSED

R(+/-) = 0.000000 OHM	R(+) = 0.000000 OHM	R(-) = 30.724117 OHM
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3. V30-12.12

Test B: output impedance when transmitting a binary zero, negative pulses into a 50R load, restricted power at 32V

double pulses into 50R (R+,R-,R+-)
isolated pulses (R-) w. loop

Conformance PASSED

R(+/-) = 0.000000 OHM	R(+) = 30.503540 OHM	R(-) = 0.000000 OHM
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4. V30-12.16

Test B: output impedance when transmitting a binary zero, positive pulses into a 400 OHM load, restricted power at 32V

double pulses into 400 OHM (R+,R-,R+-)
isolated pulses (R+) w. loop

Conformance PASSED

R(+/-) = 0.000000 OHM	R(+) = 0.000000 OHM	R(-) = 34.971443 OHM
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5. V30-12.20

Test B: output impedance when transmitting a binary zero, negative pulses into a 400R load, restricted power at 32V

double pulses into 400R (R+,R-,R+-)
isolated pulses (R-) w. loop

Conformance PASSED

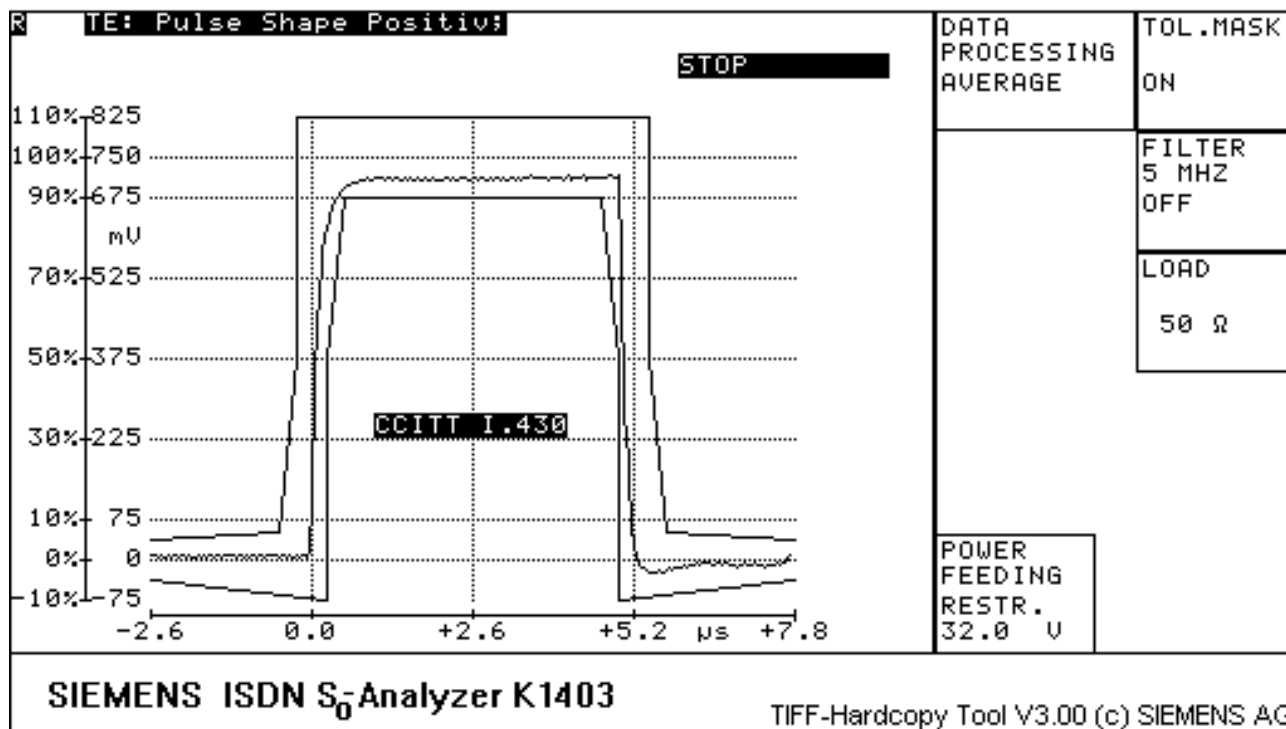
R(+/-) = 0.000000 OHM	R(+) = 34.011055 OHM	R(-) = 0.000000 OHM
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Pulse shape and amplitude

6. V30-13.4A

Pulse shape and amplitude for positive pulses, restricted power at 32V

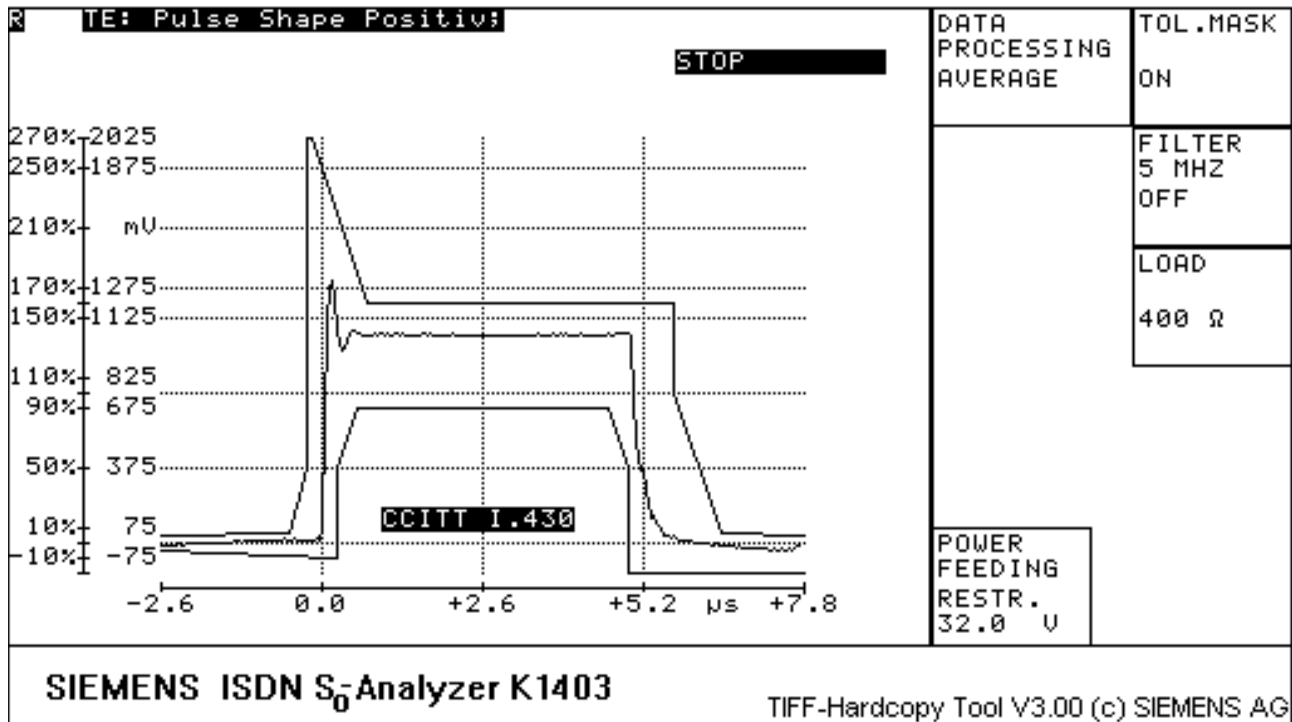
Conformance PASSED



8. V30-13.12

Test A: Voltage on a 400R load (pulse shape) for positive pulses, restricted power at 32V

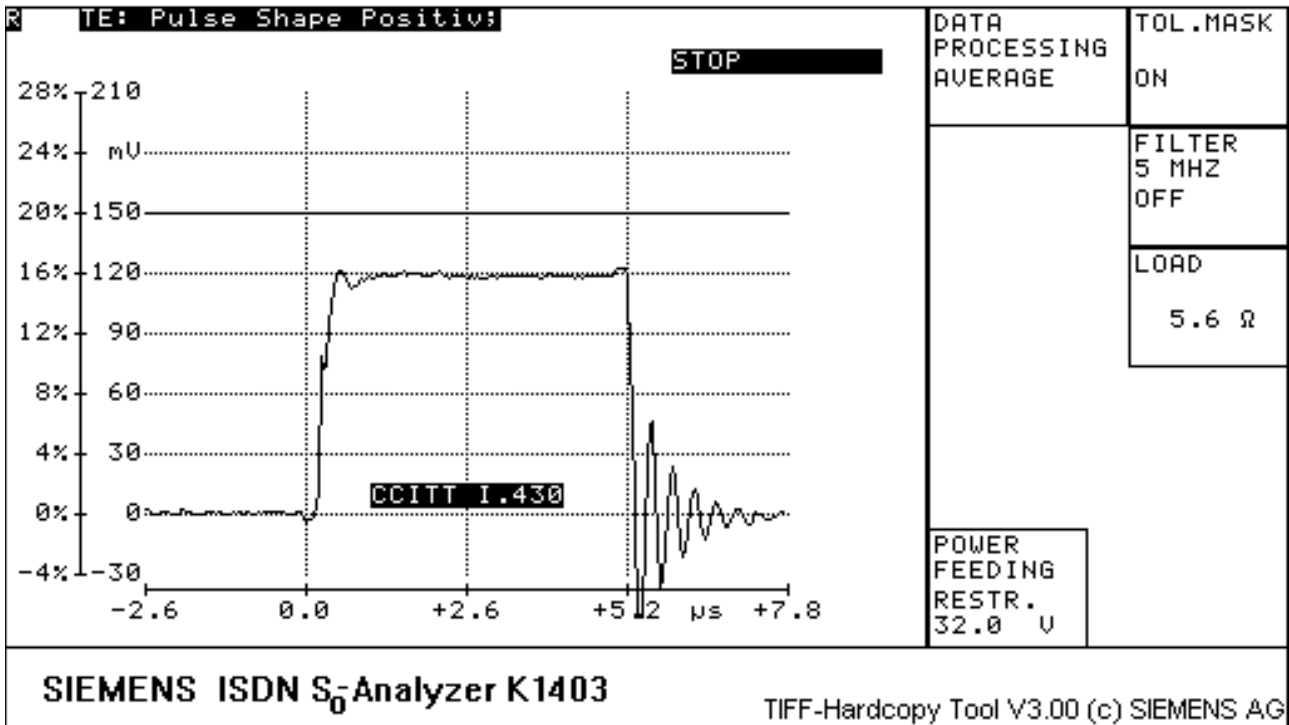
Conformance PASSED



11. V30-13.20A

Test B: Voltage on a 5.6R load (pulse shape) for positive pulses, restricted power at 32V

Conformance PASSED



15. V30-14.4

Pulse amplitude, restricted power at 32V

Conformance PASSED

$dU+/U_{nom} = -5.148371$ %	$dU-/U_{nom} = -4.874905$ %		
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18. V30-14.8

Pulse unbalance of an isolated couple of pulses, restricted power at 32V

Conformance PASSED

$df/F_{nom} = -0.487329$ %	
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Input to output offset

config. I all binary ones

Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an in put sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. I

1. V30-11.4a

Conformance PASSED

tmin = -0.146405 %	tmax = 3.853604 %
tava = 1.453641 %	

2. V30-11.4b

Conformance PASSED

tmin = -0.546384 %	tmax = 3.853604 %
tava = 2.253628 %	

3. V30-11.4c

Conformance PASSED

tmin = -0.546384 %	tmax = 3.853604 %
tava = 1.053616 %	

4. V30-11.4d

Conformance PASSED

tmin = -1.746396 %	tmax = 3.853604 %
tava = 2.253628 %	

config. II all binary ones

Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. II

5. V30-11.8a

Conformance PASSED

tmin = 0.788022 %	tmax = 8.788033 %	tava = 7.188031 %
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6. V30-11.8b

Conformance PASSED

tmin = 2.188024 %	tmax = 8.588031 %	tava = 7.388022 %
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7. V30-11.8c

tmin = 0.588020 %	tmax = 8.588031 %	tava = 7.788018 %
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8. V30-11.8d

Conformance PASSED

tmin = 2.388026 %	tmax = 8.788033 %	tava = 5.588027 %
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config. IV all binary ones

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. IV

9. V30-11.20a

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 9.838424 %
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10. V30-11.20b

Conformance PASSED

tmin = 7.038417 %	tmax = 10.638413 %	tava = 8.638415 %
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11. V30-11.20c

Conformance PASSED

tmin = 7.038417 %	tmax = 10.638413 %	tava = 8.238420 %
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12. V30-11.20d

Conformance PASSED

tmin = 3.438416 %	tmax = 10.638413 %	tava = 8.238420 %
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config. I frames with the octet 0AAH

Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D-and D-Echo channels, restricted power at 32V

[SIM-HC]
config. I

13. V30-11.24a

Conformance PASSED

tmin = -0.746365 %	tmax = 3.253659 %
tava = 2.053647 %	

Measurement finished. Expected TAV - count reached.

14. V30-11.24b

Conformance PASSED

tmin = -0.746365 %	tmax = 3.253659 %
tava = 0.853635 %	

Measurement finished. Expected TAV - count reached.

15. V30-11.24c

Conformance PASSED

tmin = -1.146374 %	tmax = 3.253659 %
tava = 1.653622 %	

Measurement finished. Expected TAV - count reached.

16. V30-11.24d

Conformance PASSED

tmin = -2.146405 %	tmax = 3.453641 %
tava = 0.653592 %	

Measurement finished. Expected TAV - count reached.

config. II frames with the octet 0AAH

Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V

config. II

17. V30-11.28a

Conformance PASSED

tmin = 4.588016 %	tmax = 8.588031 %	tava = 7.388022 %
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18. V30-11.28b

Conformance PASSED

tmin = 2.188024 %	tmax = 8.588031 %	tava = 6.188014 %
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19. V30-11.28c

Conformance PASSED

tmin = 0.788022 %	tmax = 8.788033 %	tava = 8.388015 %
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20. V30-11.28d

Conformance PASSED

tmin = 0.788022 %	tmax = 8.788033 %	tava = 7.188031 %
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config. IV frames with the octet 0AAH

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V

config. IV

21. V30-11.40a

Conformance PASSED

tmin = 7.038417 %	tmax = 10.638413 %	tava = 8.238420 %
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22. V30-11.40b

Conformance PASSED

tmin = 3.438416 %	tmax = 10.638413 %	tava = 9.838424 %
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23. V30-11.40c

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 9.438429 %
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24. V30-11.40d

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 8.238420 %
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config. I frames with all binary zeroes

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config. I

25. V30-11.44a

Conformance PASSED

tmin = -0.746365 %	tmax = 3.653622 %
tava = 1.653622 %	

26. V30-11.44b

Conformance PASSED

tmin = -0.746365 %	tmax = 3.253659 %
tava = 1.653622 %	

27. V30-11.44c

Conformance PASSED

tmin = -0.146405 %	tmax = 3.453641 %
tava = 0.253629 %	

28. V30-11.44d

Conformance PASSED

tmin = -2.146405 %	tmax = 3.453641 %
tava = 0.653592 %	

config.II frames with all binary zeroes

Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config.II

29. V30-11.48a

Conformance PASSED

tmin = 0.788022 %	tmax = 8.788033 %	tava = 6.388017 %
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30. V30-11.48b

Conformance PASSED

tmin = 0.788022 %	tmax = 8.388015 %	tava = 7.988021 %
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31. V30-11.48c

Conformance PASSED

tmin = -0.011967 %	tmax = 8.388015 %
tava = 7.588025 %	

32. V30-11.48d

Conformance PASSED

tmin = 0.588020 %	tmax = 8.188012 %	tava = 6.988029 %
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config. IV frames with all binary zeroes

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config. IV

33. V30-11.60a

Conformance PASSED

tmin = 5.838432 %	tmax = 10.638413 %	tava = 8.238420 %
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34. V30-11.60b

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 9.038434 %
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35. V30-11.60c

Conformance PASSED

tmin = 3.438416 %	tmax = 10.638413 %	tava = 8.638415 %
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36. V30-11.60d

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 7.438431 %
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config. I frames with a 219-1 PRBS

Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config. I

37. V30-11.64a

Conformance PASSED

tmin = -0.946393 %	tmax = 4.253629 %
tava = 0.653592 %	

38. V30-11.64b

Conformance PASSED

tmin = -0.946393 %	tmax = 4.253629 %
tava = 2.653592 %	

39. V30-11.64c

Conformance PASSED

tmin = -1.146374 %	tmax = 3.653622 %
tava = 1.653622 %	

40. V30-11.64d

Conformance PASSED

tmin = -2.746365 %	tmax = 3.653622 %
tava = 0.853635 %	

config. II frames with a 219-1 PRBS

Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config. II

41. V30-11.68a

Conformance PASSED

tmin = 0.788022 %	tmax = 8.788033 %	tava = 6.788035 %
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42. V30-11.68b

Conformance PASSED

tmin = -0.611989 %	tmax = 8.588031 %
tava = 4.988030 %	

43. V30-11.68c

Conformance PASSED

tmin = 2.188024 %	tmax = 8.588031 %	tava = 5.788020 %
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44. V30-11.68d

Conformance PASSED

tmin = -0.211970 %	tmax = 8.588031 %
tava = 7.388022 %	

config.IV frames with a 219-1 PRBS

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config.IV

45. V30-11.80a

Conformance PASSED

tmin = 5.838432 %	tmax = 10.638413 %	tava = 8.638415 %
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46. V30-11.80b

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 9.838424 %
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47. V30-11.80c

Conformance PASSED

tmin = 4.238429 %	tmax = 10.638413 %	tava = 9.838424 %
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48. V30-11.80d

Conformance PASSED

tmin = 3.438416 %	tmax = 10.638413 %	tava = 9.438429 %
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Jitter characteristics

config. III binary ones in D, D-Echo and both B channels

1. V30-10.12

Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. IIIa

UI(pp) = 4.700000 %	UI(rms) = 1.000000 %
UI(pp-Hold) = 4.900000 %	

2. V30-10.16

Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. IIIb

UI(pp) = 4.700000 %	UI(rms) = 1.000000 %
UI(pp-Hold) = 4.800000 %	

config. III frames with continuous octets of 0AAH

3. V30-10.32

Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels and continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config. IIIa

UI(pp) = 3.900000 %	UI(rms) = 0.900000 %
UI(pp-Hold) = 3.900000 %	

4. V30-10.36

Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels and continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, -Echo and both B channels, restricted power at 32V

config. IIIb

UI(pp) = 4.700000 %	UI(rms) = 0.900000 %
UI(pp-Hold) = 4.700000 %	

config. III frames with a 219-1 PRBS

5. V30-10.52

Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config. IIIa

UI(pp) = 5.300000 %	UI(rms) = 1.100000 %
UI(pp-Hold) = 5.300000 %	

6. V30-10.56

Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config. IIIb

UI(pp) = 5.400000 %	UI(rms) = 1.100000 %
UI(pp-Hold) = 5.500000 %	

config. I binary ones in D, D-Echo and both B channels
1. V30-10.4

Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. I

UI(pp) = 5.500000 %	UI(rms) = 1.100000 %
UI(pp-Hold) = 5.900000 %	

config. II binary ones in D, D-Echo and both B channels
2. V30-10.8

Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. II

UI(pp) = 4.700000 %	UI(rms) = 1.000000 %
UI(pp-Hold) = 5.000000 %	

config. IV binary ones in D, D-Echo and both B channels
3. V30-10.20

Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V

config. IV

UI(pp) = 4.700000 %	UI(rms) = 1.100000 %
UI(pp-Hold) = 4.700000 %	

config. I frames with continuous octets of 0AAH
4. V30-10.24

Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels and continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config. I

UI(pp) = 5.300000 %	UI(rms) = 0.900000 %
UI(pp-Hold) = 5.700000 %	

config. II frames with continuous octets of 0AAH

5. V30-10.28

Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config. II

UI(pp) = 4.600000 %	UI(rms) = 0.900000 %
UI(pp-Hold) = 4.700000 %	

config. IV frames with continuous octets of 0AAH

6. V30-10.40

Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V

config. IV

UI(pp) = 4.600000 %	UI(rms) = 1.000000 %
UI(pp-Hold) = 4.700000 %	

config. I frames with a 219-1 PRBS

7. V30-10.44

Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config. I

UI(pp) = 6.800000 %	UI(rms) = 1.100000 %
UI(pp-Hold) = 7.200000 %	

config. II frames with a 219-1 PRBS

8. V30-10.48

Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 219-1PRBS in D, D-Echo and both B channels, restricted power at 32V

config. II

UI(pp) = 5.400000 %	UI(rms) = 1.100000 %
UI(pp-Hold) = 5.400000 %	

config. IV frames with a 219-1 PRBS

9. V30-10.60

Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, restricted power at 32V

config. IV

UI(pp) = 4.900000 %	UI(rms) = 1.000000 %
UI(pp-Hold) = 5.000000 %	

Receiver sensitivity

config. I

1. V30-17.4a

Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

2. V30-17.4b

Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

3. V30-17.4c

Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0

time = 60.000000 s

4. V30-17.4d

Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

5. V30-17.8a

Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

6. V30-17.8b

Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

7. V30-17.8c

Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

config.II

8. V30-17.8d

Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. I

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

9. V30-17.12a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

10. V30-17.12b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

11. V30-17.12c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

12. V30-17.12d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

13. V30-17.16a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

14. V30-17.16b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

15. V30-17.16c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

16. V30-17.16d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.II

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

config. IV

17. V30-17.36a

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IV

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

18. V30-17.36b

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IV

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

19. V30-17.36c

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IV

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

20. V30-17.36d

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IV

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

config.IIIa

1. V30-17.20a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

2. V30-17.20b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

3. V30-17.20c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

4. V30-17.20d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

5. V30-17.24a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

6. V30-17.24b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

7. V30-17.24c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

8. V30-17.24d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μ s delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config.IIIa

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

config.IIIb

9. V30-17.28a

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

10. V30-17.28b

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

11. V30-17.28c

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

12. V30-17.28d

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

13. V30-17.32a

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

14. V30-17.32b

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

15. V30-17.32c

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1

ErroredIntervals = 0
time = 60.000000 s

16. V30-17.32d

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 32V

with integrated jitter generator
config. IIIb

Conformance PASSED

BitErrorCount = 0.000000
BitErrorRate = 0.000000
Intervals = 1
ErroredIntervals = 0
time = 60.000000 s

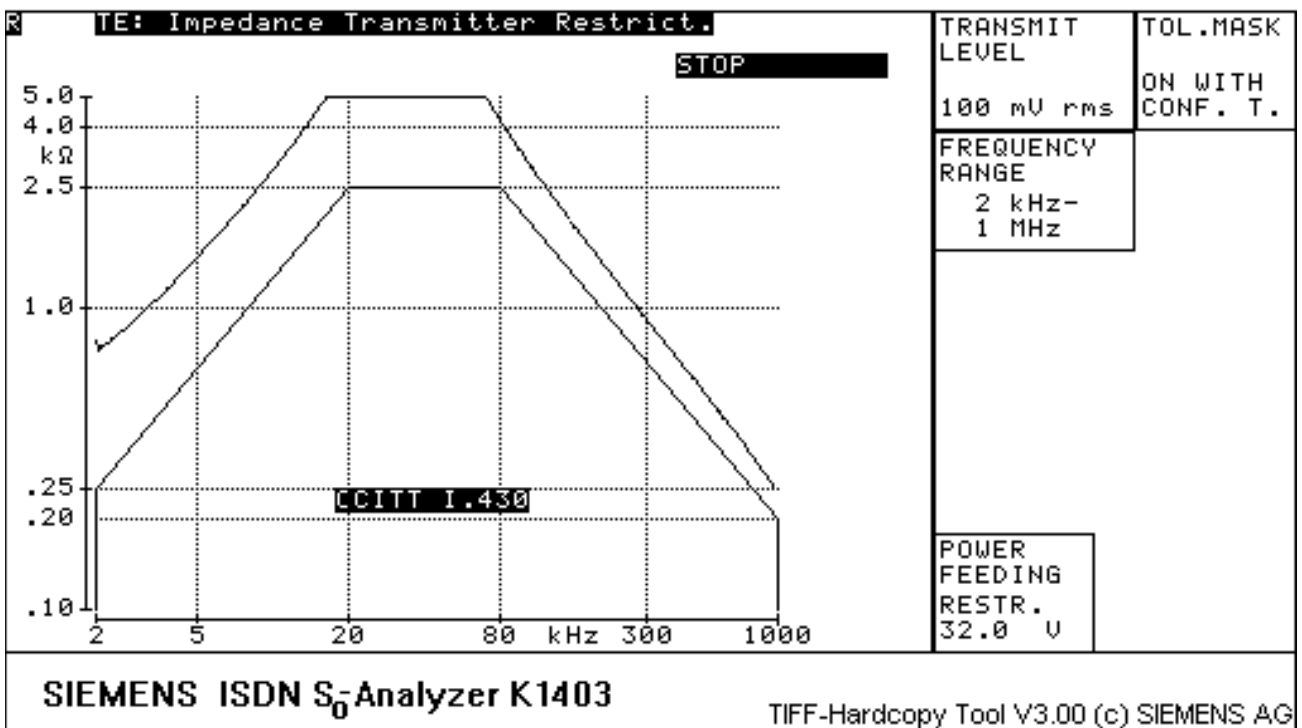
SA3 with HFC-SP 3V3 operation

Impedance Transmitter

1. V30-12.4

Test A: output impedance when transmitting a binary one in state F3, restricted power at 32V

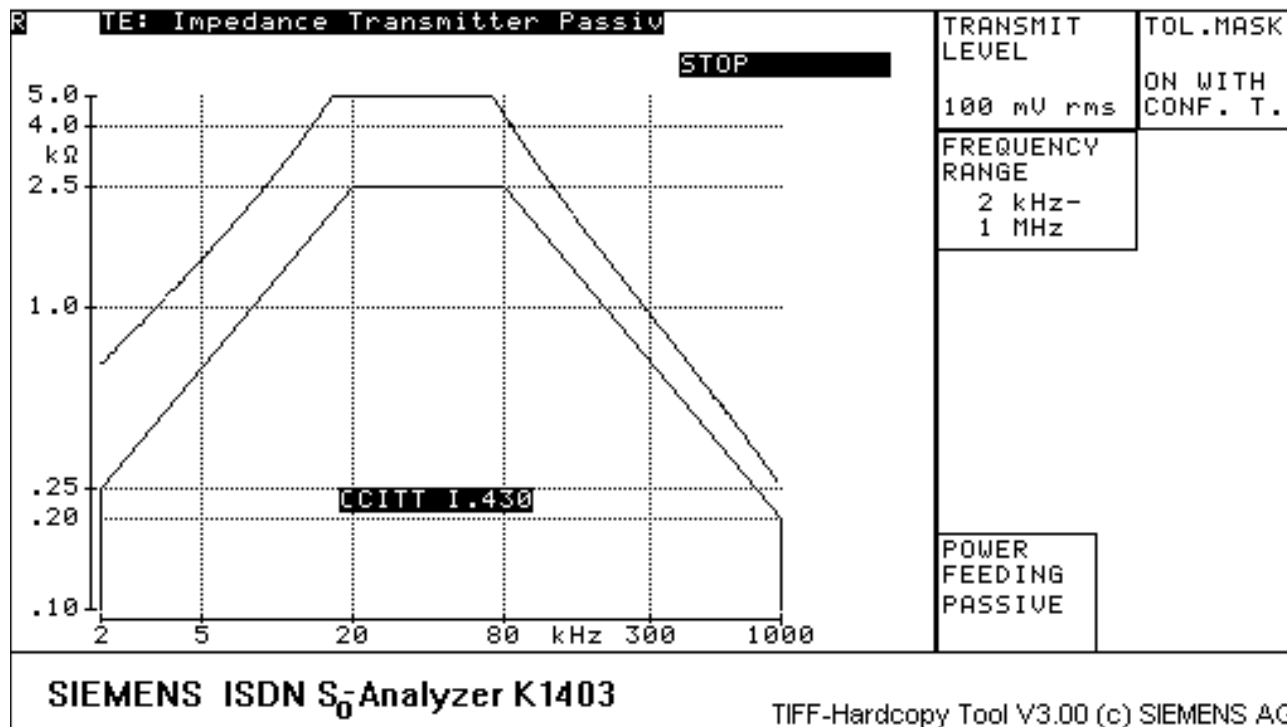
Conformance PASSED



29. V30-12.25

Test D: output impedance when transmitting a binary one in state F1

Conformance PASSED

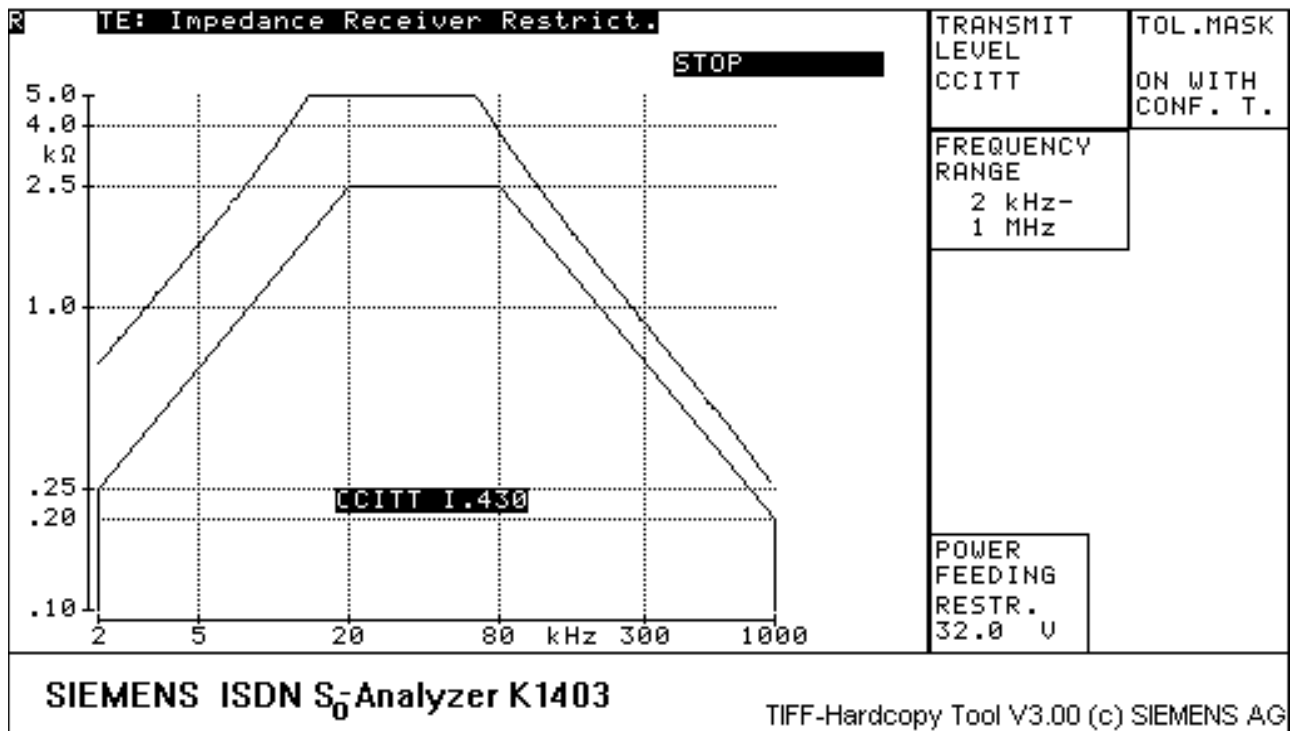


Impedance Receiver

24. V30-16.4

Test A: Receiver input impedance in state F3, restricted power at 32V

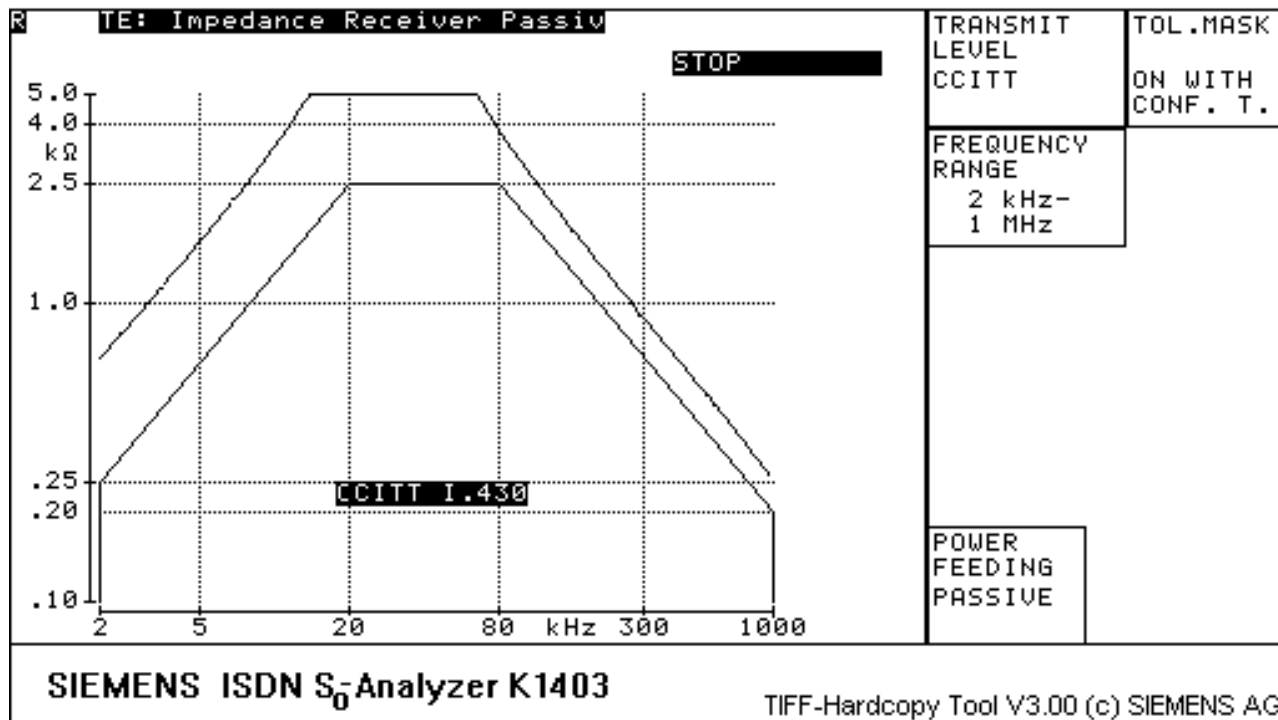
Conformance PASSED



31. V30-16.9

Test C: Receiver input impedance in state F1

Conformance PASSED

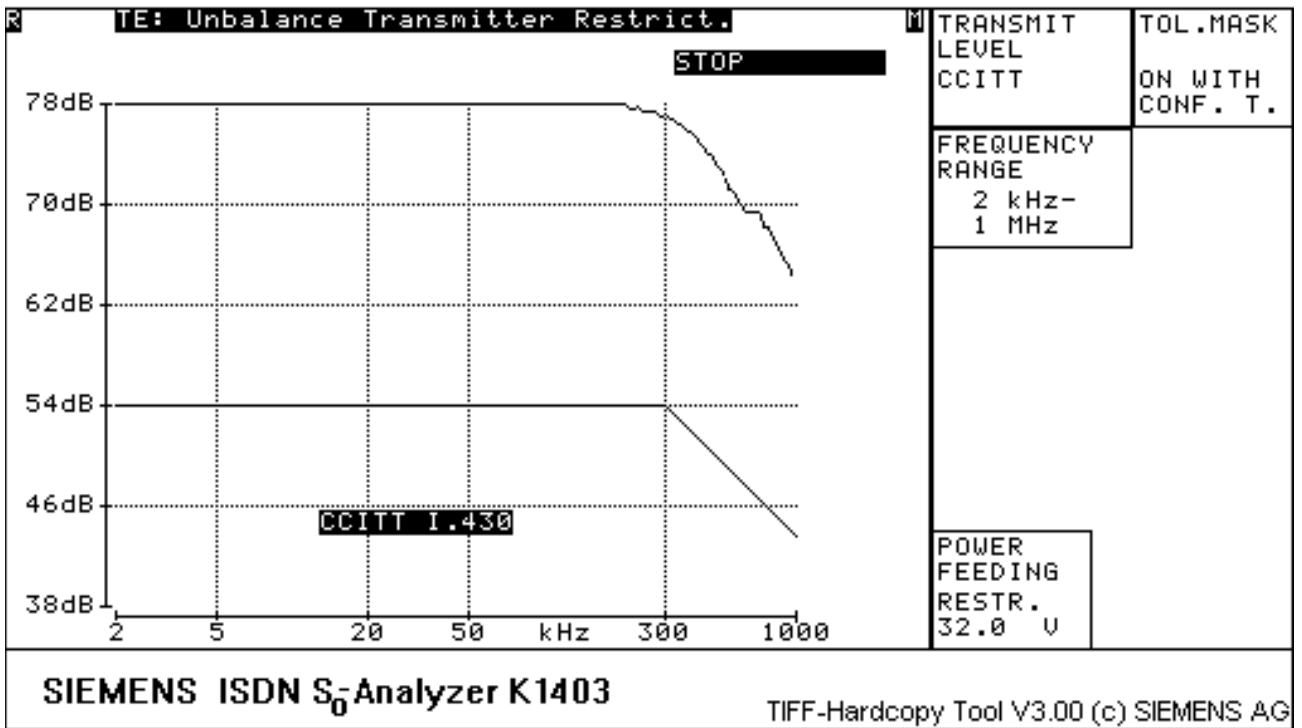


Transmitter output longitudinal conversion loss

22. V30-15.4

Transmitter output longitudinal conversion loss in state F3, restricted power at 32V

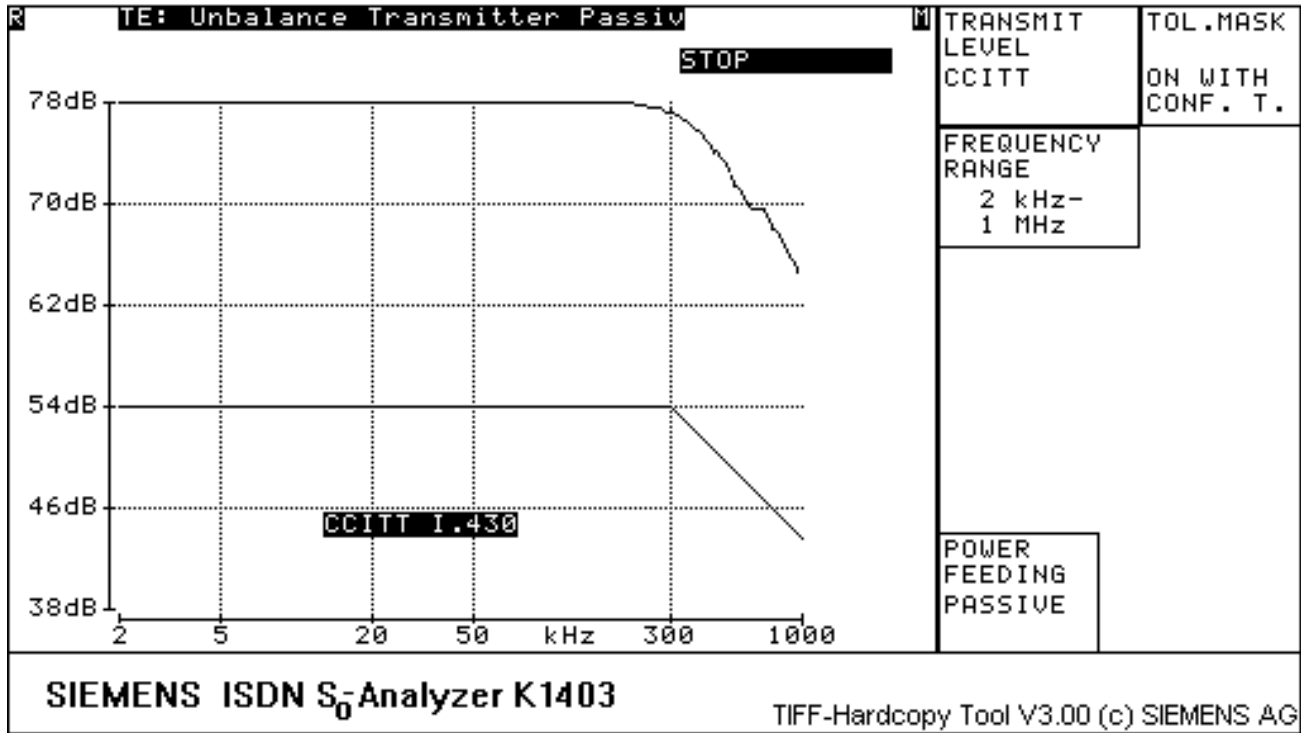
Conformance PASSED



30. V30-15.5

Transmitter output longitudinal conversion loss in state F1

Conformance PASSED

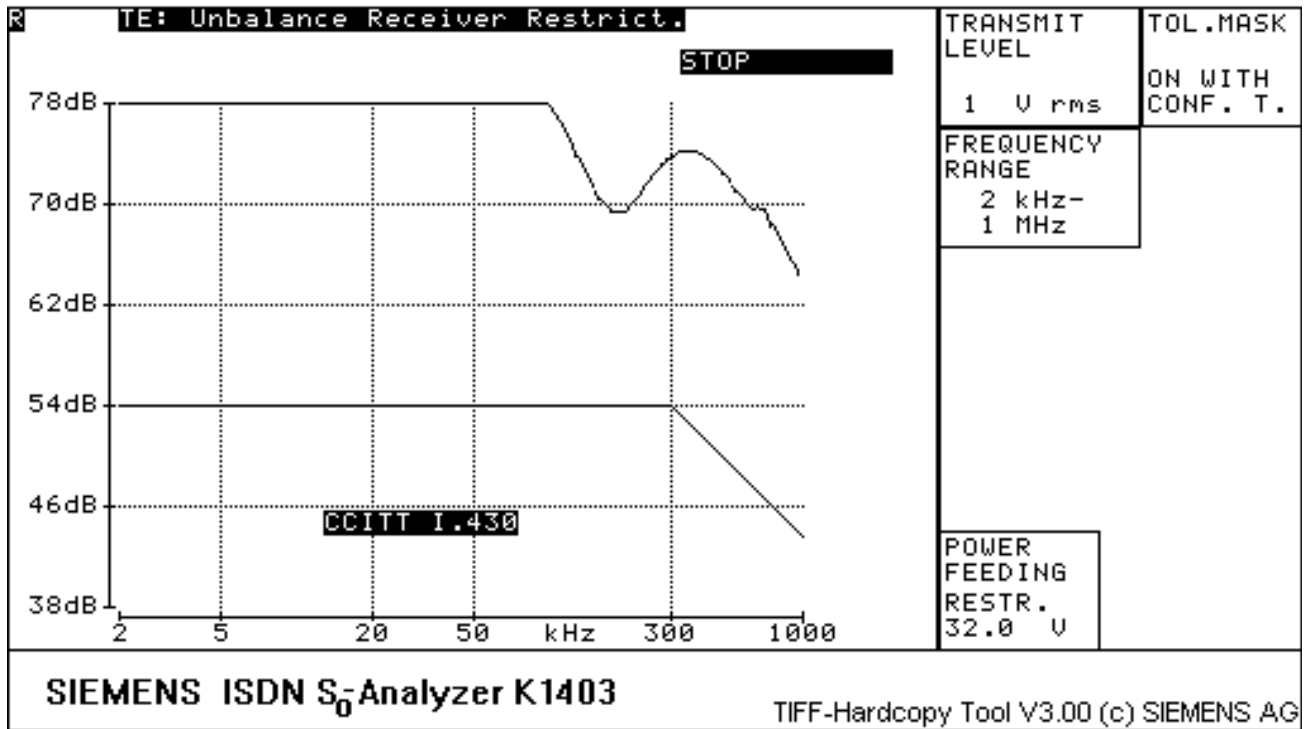


Receiver unbalance about earth

28. V30-18.4U

Receiver unbalance about earth (longitudinal conversion loss) in state F3, restricted power at 32V

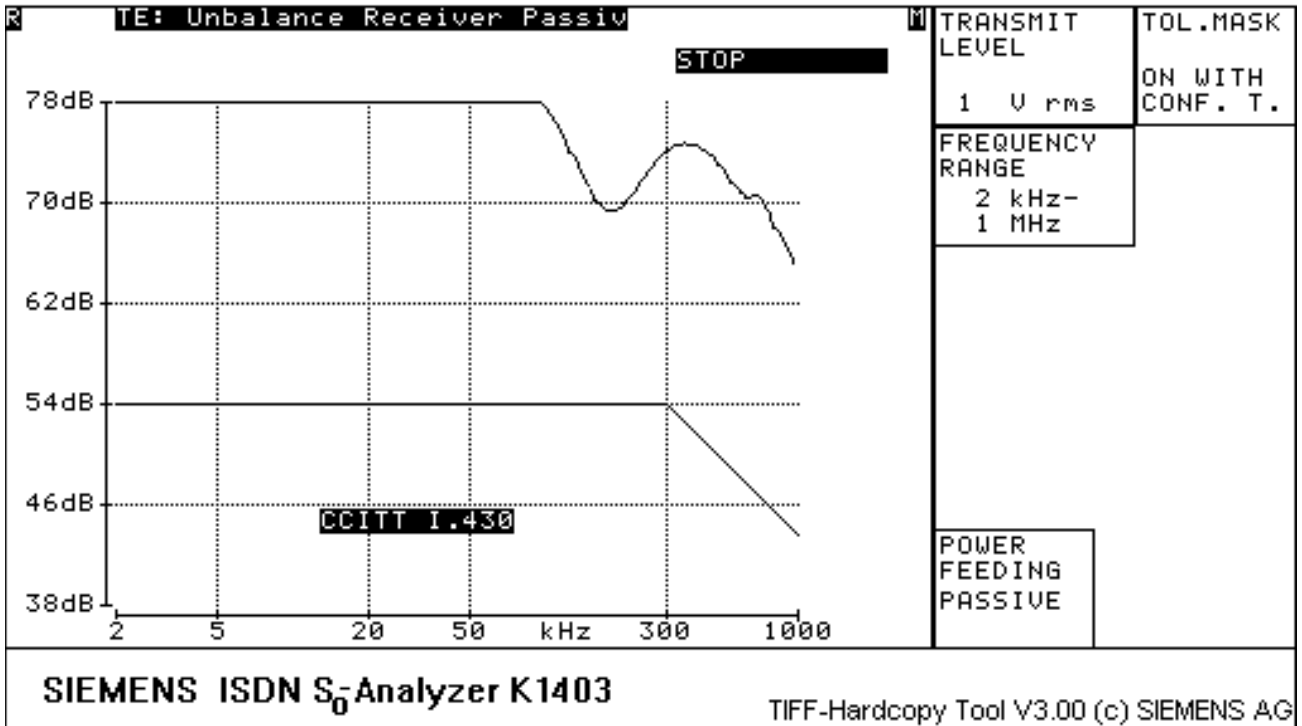
Conformance PASSED



32. V30-18.5U

Receiver unbalance about earth (longitudinal conversion loss) in state F1

Conformance PASSED



output impedance

2. V30-12.8

Test B: output impedance when transmitting a binary zero, positive pulses into a 50R load, restricted power at 32V

double pulses into 50R (R+,R-,R+-)
isolated pulses (R+) w. loop

Conformance PASSED

R(+/-) = 0.000000 OHM	R(+) = 0.000000 OHM	R(-) = 29.268250 OHM
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3. V30-12.12

Test B: output impedance when transmitting a binary zero, negative pulses into a 50R load, restricted power at 32V

double pulses into 50R (R+,R-,R+-)
isolated pulses (R-) w. loop

Conformance PASSED

R(+/-) = 0.000000 OHM	R(+) = 29.052647 OHM	R(-) = 0.000000 OHM
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4. V30-12.16

Test B: output impedance when transmitting a binary zero, positive pulses into a 400 OHM load, restricted power at 32V

double pulses into 400 OHM (R+,R-,R+-)
isolated pulses (R+) w. loop

Conformance PASSED

R(+/-) = 0.000000 OHM	R(+) = 0.000000 OHM	R(-) = 32.950439 OHM
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5. V30-12.20

Test B: output impedance when transmitting a binary zero, negative pulses into a 400R load, restricted power at 32V

double pulses into 400R (R+,R-,R+-)
isolated pulses (R-) w. loop

Conformance PASSED

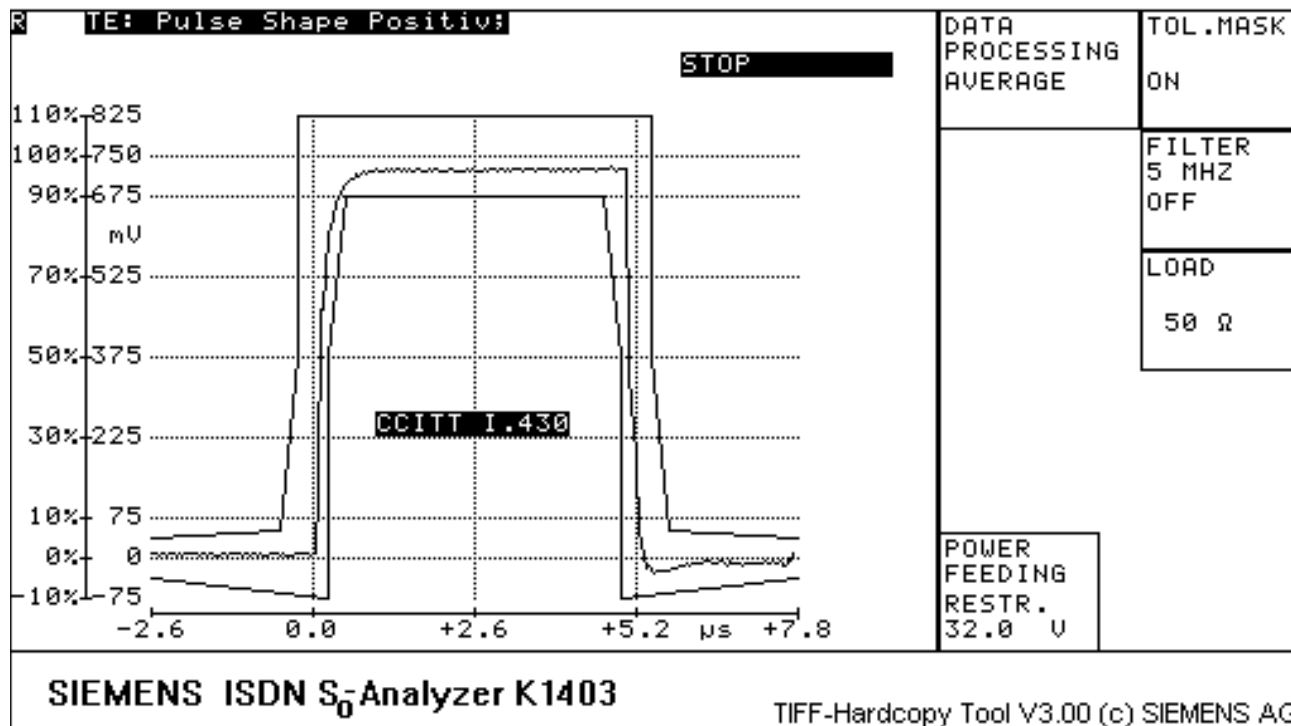
R(+/-) = 0.000000 OHM	R(+) = 31.182671 OHM	R(-) = 0.000000 OHM
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Pulse shape and amplitude

6. V30-13.4A

Pulse shape and amplitude for positive pulses, restricted power at 32V

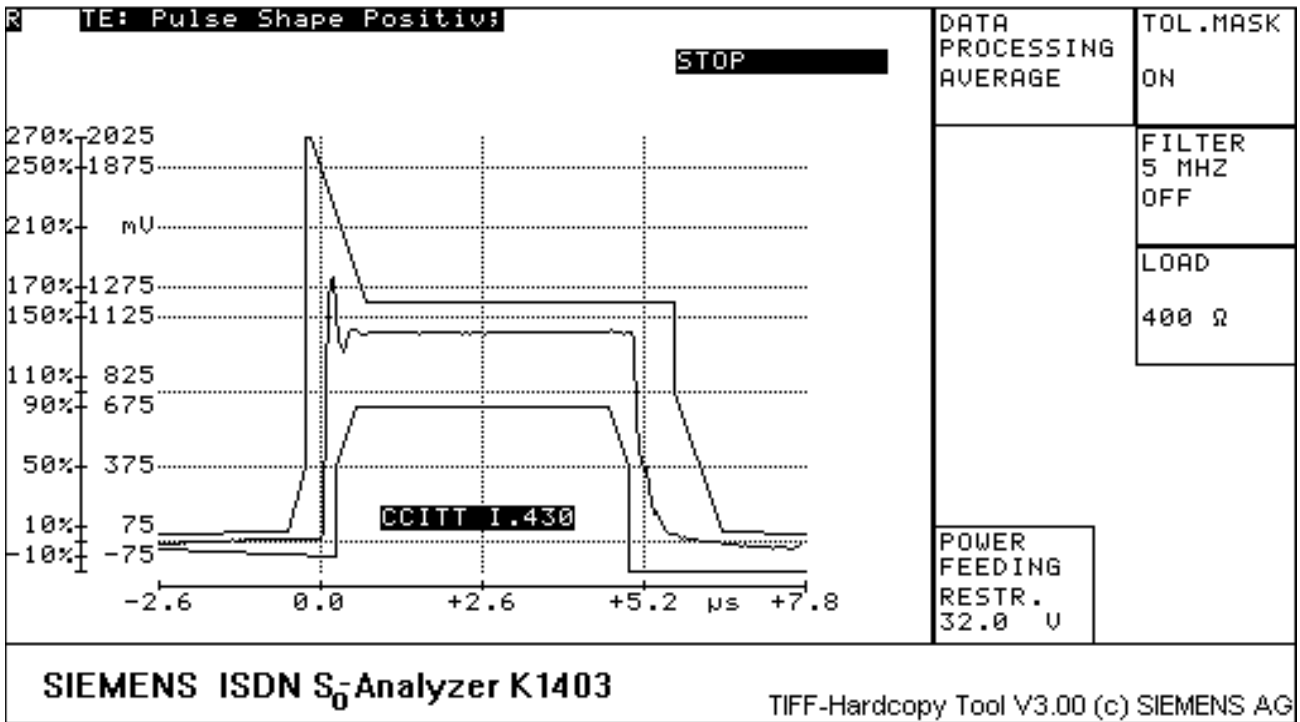
Conformance PASSED



8. V30-13.12

Test A: Voltage on a 400R load (pulse shape) for positive pulses, restricted power at 32V

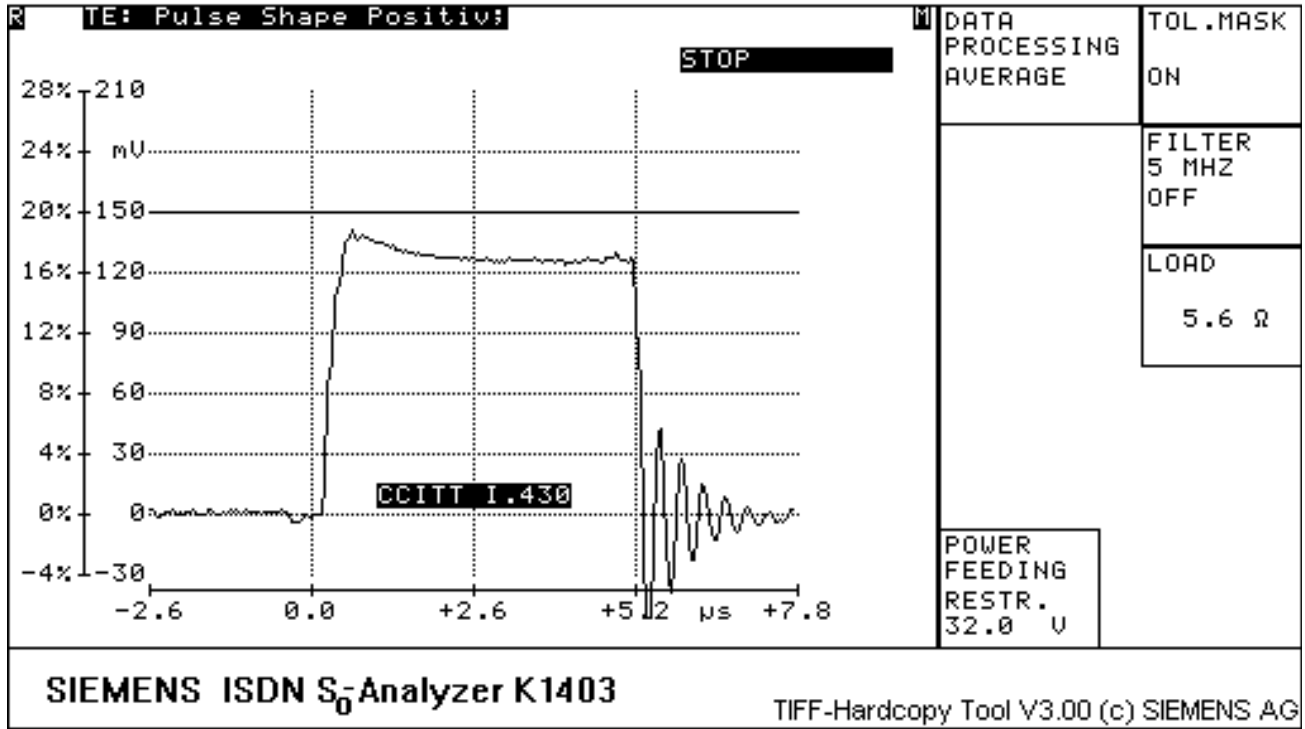
Conformance PASSED



11. V30-13.20A

Test B: Voltage on a 5.6R load (pulse shape) for positive pulses, restricted power at 32V

Conformance PASSED



15. V30-14.4

Pulse amplitude, restricted power at 32V

Conformance PASSED

dU+/Unom = -3.722906 %	dU-/Unom = -3.672488 %		
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Input to output offset

config.IV

1. V30-11.78d

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, normal power at 24V

config.IV

Conformance PASSED

tmin = 3.038421 %	tmax = 11.038432 %	tava = 7.438431 %
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config. I

2. V30-11.62d

Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 219-1 PRBS in D, D-Echo and both B channels, normal power at 42V

[SIM-HC]
config. I

Conformance PASSED

tmin = -1.146374 %	tmax = 4.453610 %
tava = 1.653622 %	