

Lead Free HFC-S PCI A Product Change Notification

Lead-free Package

Cologne Chip's leaded HFC-S PCI A is replaced by a lead-free version. Pinning of lead-free HFC-S PCI A remains the same. It is assured that existing PCB layouts do not require any adaption.

Also the part number of lead-free HFC-S PCI A remains unchanged, but the new version can be clearly identified by week code: Week codes dated later than 2004-30 reveal lead-free ICs (chip marking code: YYWW, e.g. 0430). The commonly used logos for "Pb-free" and "RoHS compliant" are printed next to the part number barcodes on the Cologne Chip bag label (see Illustration 1).

Moreover there is a marking on the label of the outer chip box, which indicates lead-free microchips: a capital „G“ is hyphenated to the product name, e.g. „HFC-SPCIA“ becomes „HFC-SPCIA-G“ showing that it is a „Green“ product.

Qualification

QFP100 packages of HFC-S PCI A have MSL3 classification (Moisture Sensitivity Level 3) and comply basically with the most current JEDEC JSTD-020C standard (more detailed information on these standards is available upon request). Moreover lead-free HFC-S PCI A is fully RoHS compliant.

Solder Reflow Profile for lead-free HFC-S PCI A

Often the same equipment set and process steps used for leaded soldering can be used for lead-free soldering. However for lead-free soldering of HFC-S PCI A there are some important facts that must be taken into account as the material set used for lead-free soldering is different and higher reflow temperatures are required. Lead-free solder typically melts at a temperature 35°C higher than traditional tin/lead solder. Therefore two important differences in solder reflow profile are the higher melting temperature at 217°C as well as higher peak reflow temperature at 260°C.

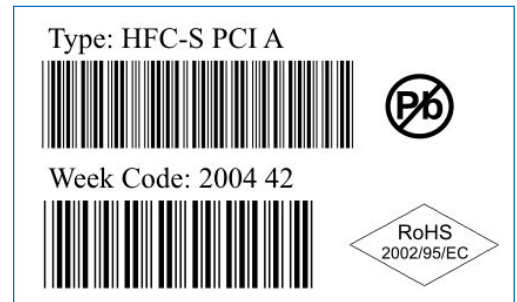
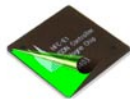


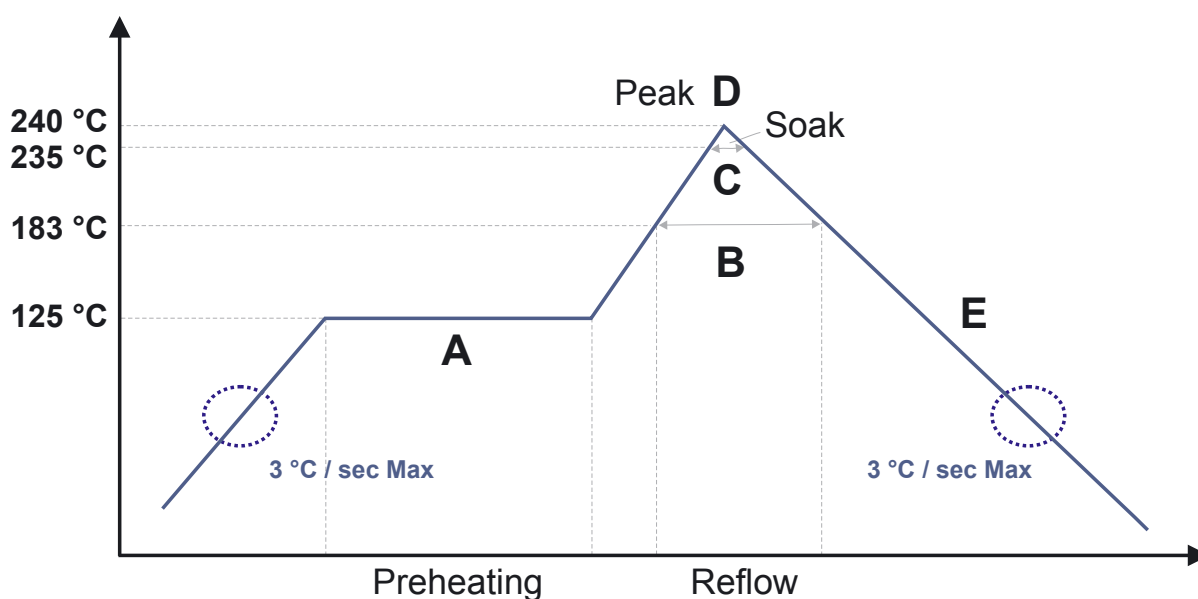
Illustration 1: Bag label for Pb-free products



The profile of **Sn-Pb eutectic** packages is described in Table 1. Please take note of the characteristic process sections that are also displayed in Graph 1.

Section	Sn-Pb Eutectic Package	
	Temperature (°C)	Time (second)
Ramp-up rate	3°C/second max.	
A: Preheating	125 +/- 25	90 +/- 30
B: Reflow	183	105 +/- 20% (84 - 126)
C: Soak	235 +5	20 +/- 20% (16 - 24)
D: Peak	240 +0/-5	
E: Ramp-down rate	3°C/second max.	

Table 1: Soldering Reflow Conditions for Sn-Pb Eutectic Package



Graph 1: Soldering Reflow Profile for Sn-Pb Eutectic Package

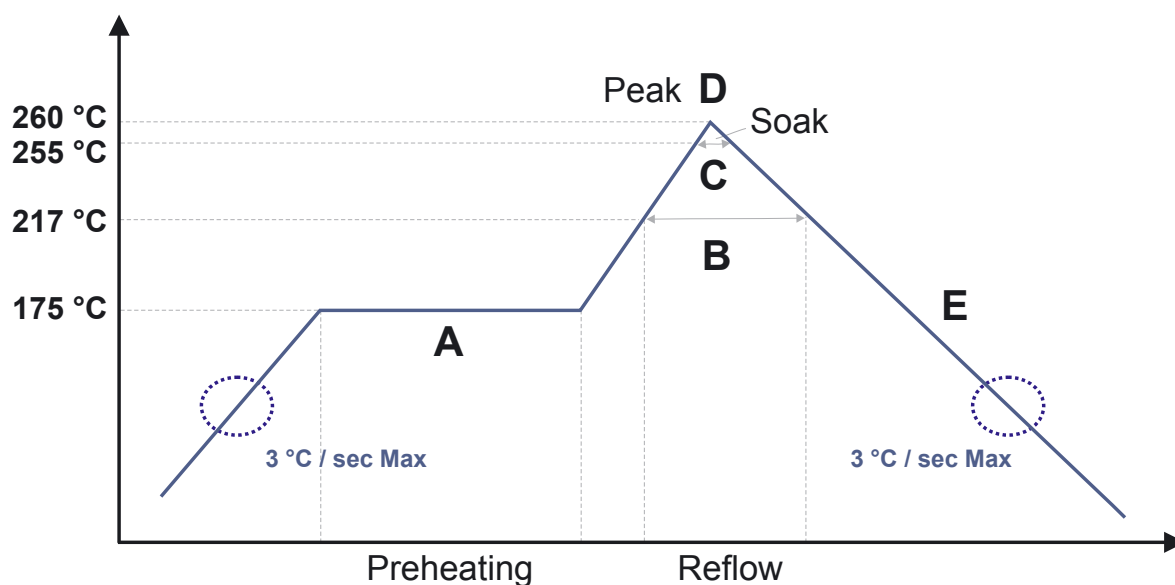
Likewise the soldering reflow profile for **Pb-free** packages is represented by Table 2 and Graph 2.

The Sn-Ag-Cu (tin-silver-copper) family of solder alloys is most commonly used for SMT manufacturing. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of components, the



Section	Pb-free Package	
	Temperature (°C)	Time (second)
Ramp-up rate	3°C/second max.	
A: Preheating	175 +/- 25	120 +/- 60
B: Reflow	217	105 +/- 20% (84 - 126)
C: Soak	255 +5	30 +/- 20% (24 - 36)
D: Peak	260 +0/-5	
E: Ramp-down rate	3°C/second max.	

Table 2: Soldering Reflow Conditions for Pb-free Package



Graph 2: Soldering Reflow Profile for Pb-free Package

mix of large and small components and the solder paste chemistry being used.

Should you require more detailed information on this issue or have any questions regarding the conversion of Cologne Chip products, please write an e-mail to support@colognechip.com We will be glad to assist.

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Relevant sources of this information can be downloaded from the following websites:

1. JEDEC JSTD-020C: <http://www.jedec.org/>