

HFC-S USB ISDN Controller

Reference Design for USB ISDN TA

March 2007

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1 Introduction

This document shows a reference design for a USB ISDN terminal adapter implemented with HFC-S USB. This circuitry can be used in TE interface mode. It fulfills all criteria of the ITU-T I.430 test specification [2].

A detailed description of the HFC-S USB microchip functions is given in the data sheet [1].

2 Reference circuitry

Figure 1 and 2 show the reference circuitry of an USB ISDN TA using HFC-S USB.

The device is powered from the USB interface. The voltage regulator U3 generates stable 3.3 V power operating voltage.

The parallel port can optionally be used for status LEDs, e.g., as shown with lines PORT_D0 .. PORT_D2 . Unused ports should be tied to ground with a pull-down resistor each. These resistors are required because several generic open source drivers use different ports for LED addressing – a common pull-down resistor for *all* ports would lead to a short circuit.

Optional capacitors C24 .. C27 are used for EMI reduction.

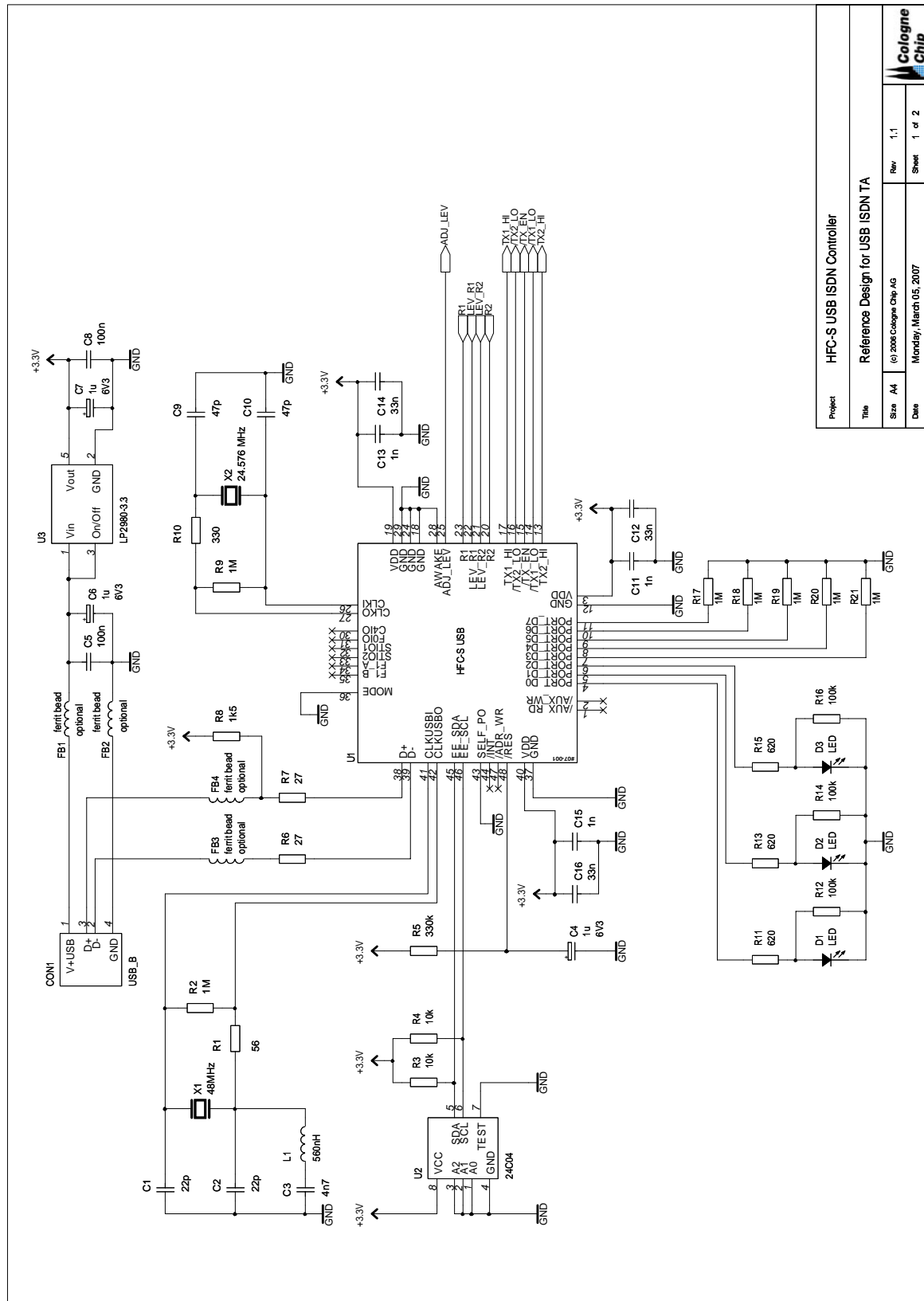


Figure 1: Reference schematic for an ISDN USB TA (page 1)

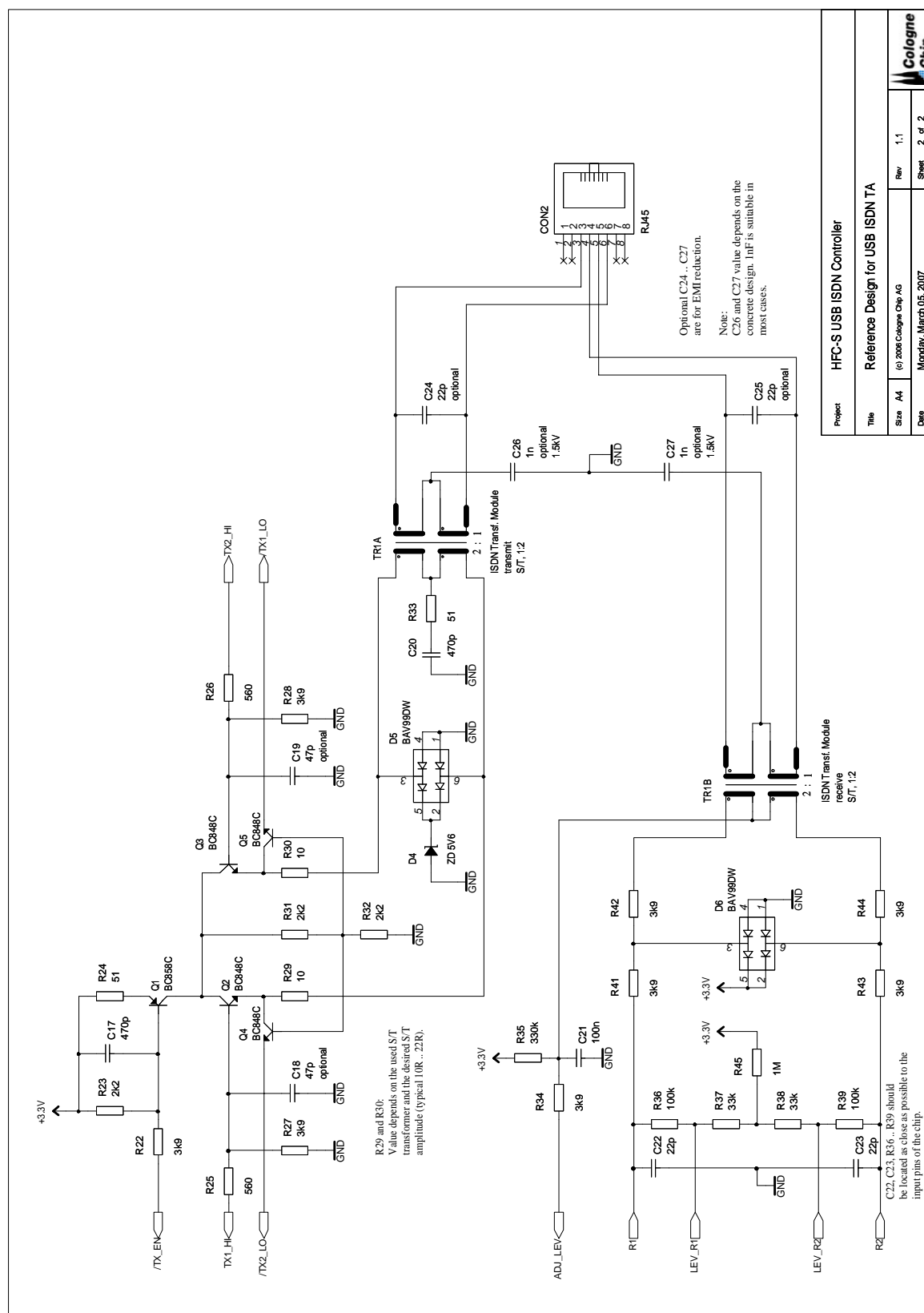


Figure 2: Reference schematic for an ISDN USB TA (page 2)

Bill of Materials: HFC-S USB ISDN Controller**Reference Design for USB ISDN TA**

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(n.p. = not populated)

Resistors (44 pcs.)

R1	56
R2,R9,R17,R18,R19,R20,R21,R45	1M
R3,R4	10k
R5,R35	330k
R6,R7	27
R8	1k5
R10	330
R11,R13,R15	620
R12,R14,R16,R36,R39	100k
R22,R27,R28,R34,R41,R42,R43,R44	3k9
R23,R31,R32	2k2
R24,R33	51
R25,R26	560
R29,R30	10
R37,R38	33k

Capacitors (21 . . 27 pcs.)

C1,C2,C22,C23	22p
C3	4n7
C4,C6,C7	1u 6V3
C5,C8,C21	100n
C9,C10	47p
C11,C13,C15	1n
C12,C14,C16	33n
C17,C20	470p
C18,C19	47p optional
C24,C25	22p optional
C26,C27	1n 1.5kV, optional

Diodes (6 pcs.)

D1,D2,D3	LED
D4	ZD 5V6
D5,D6	BAV99DW

Transistors (5 pcs.)

Q1	BC858C
Q2,Q3,Q4,Q5	BC848C

Coils/Inductors/Filters (1 . . 5 pcs.)

FB1,FB2,FB3,FB4	ferrit bead	optional
L1	560nH	

Transformers (1 pc.)

TR1	ISDN Transf. Module	S/T, 1:2
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Integrated Circuits (ICs) (3 pcs.)

U1	HFC-S USB
U2	24C04
U3	LP2980-3.3

Connectors (2 pcs.)

CON1	USB_B
CON2	RJ45

Oscillators (2 pcs.)

X1	48 MHz
X2	24.576 MHz

Total:

44 x Resistors
 21 x Capacitors
 6 x Diodes
 5 x Transistors
 1 x Coils/Inductors/Filters
 1 x Transformer
 3 x Integrated Circuits (ICs)
 2 x Connectors

83 total
 + 10 optional

3 Layout recommendations

The components which are connected to the data inputs R1 and R2 as well as to the level detection pins LEV_R1 and LEV_R2 should be located as close as possible to the HFC-S USB. Figure 3 shows a suitable layout example.

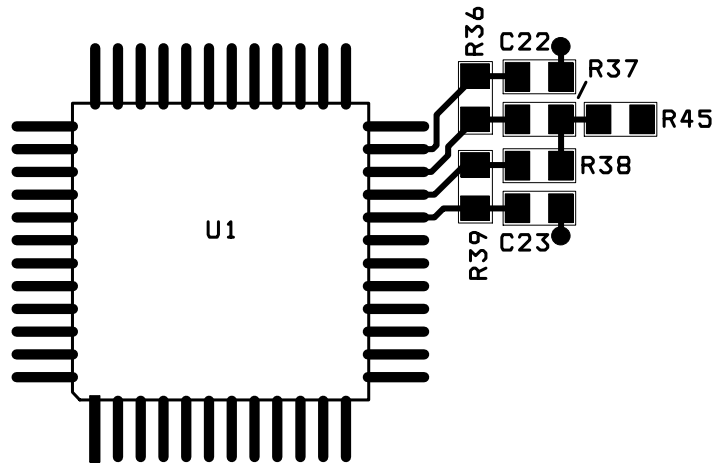


Figure 3: Layout example for the connection to the S/T interface input pins

The HFC-S USB requires three pairs of decoupling capacitor. VDD should shortly be connected over capacitor pins to the microchip like shown in Figure 4. Ground pins of HFC-S USB as well as ground connection of the decoupling capacitors need not directly be interconnected. A ground plane can optionally be used as it is suggested with vias in Figure 4.

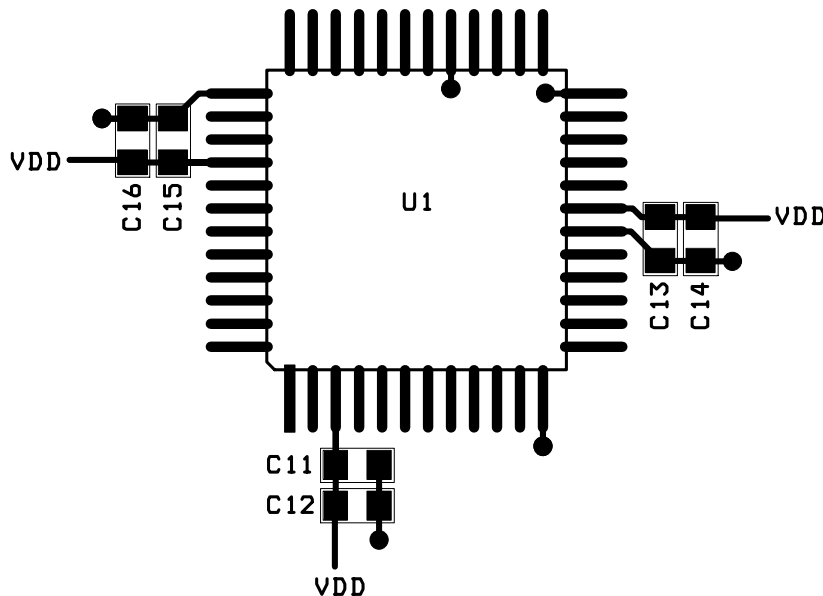


Figure 4: Layout example for the decoupling capacitors

References

- [1] Cologne Chip AG. *HFC-S USB ISDN 2BDS0, ISDN HDLC FIFO controller with S/T interface and USB interface (data sheet)*, May 2002.
- [2] Telecommunication Standardization Sector of International Telecommunication Union (ITU). *ITU-T I.430: Integrated services digital network (ISDN); ISDN user-network interfaces. Basic user-network interface – Layer 1 specification*, November 1995.

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