

GateMate™ FPGA

High-Speed Transceiver (SerDes)



Patrick Urban, M.Sc.
Research & Development
Cologne Chip AG

FPGA
CONFERENCE
EUROPE

Agenda



1. Introduction to GateMate FPGA

Architecture & Toolchain

2. Detailed look into the GateMate SerDes

Features & Tools

3. 1000BASE-X Implementation & Example

SerDes Wizard & Loopback Example

Company Overview



- 1994 Founding year of **Cologne Chip Designs GmbH**.
- 1996 Presentation of world's first single-chip-solution for ISDN.
- 2000 Rebranding to **Cologne Chip AG** and sales in millions of units after annual growth rates by 100%
- 2007 Establishment of the **XHFC-Series** with open access to drivers and software; part of Linux Kernel since v. 2.6.27.
- 2020 Introduction of a new product line: **GateMate FPGA**.



> 30 Years

Experience in
Semiconductor
Business



Certified Quality



100 %

Always on-time
Same-Day Deliveries

 designed and
manufactured
in Germany

Reliable Supply Chain

GateMate FPGA

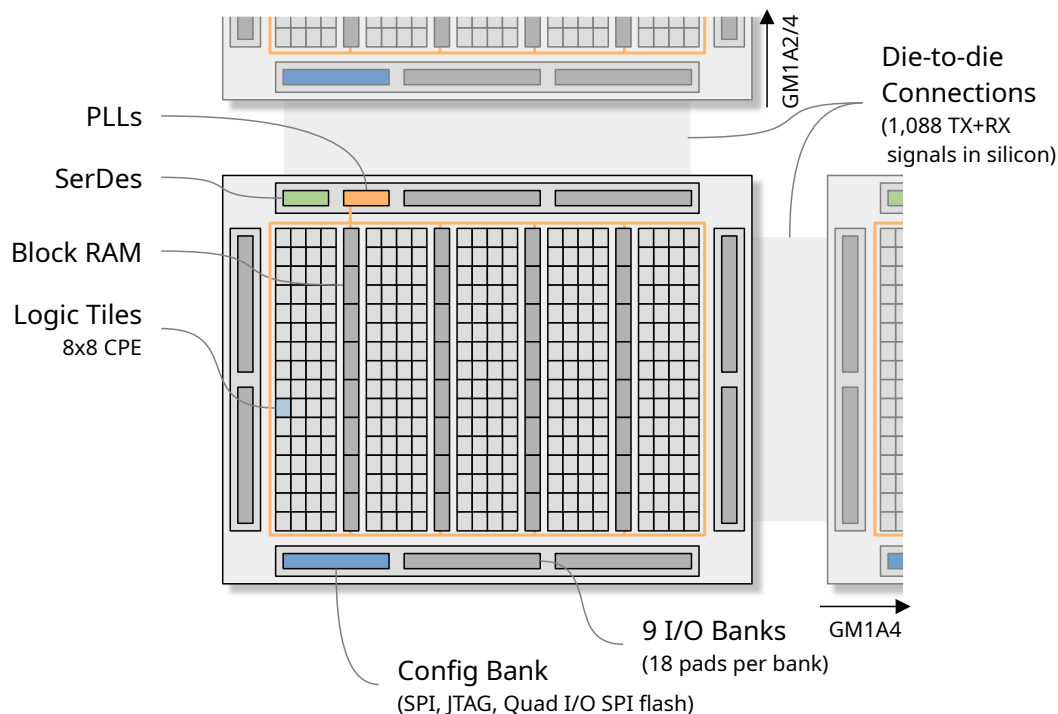
Features at a glance



FPGAs
MADE IN
GERMANY

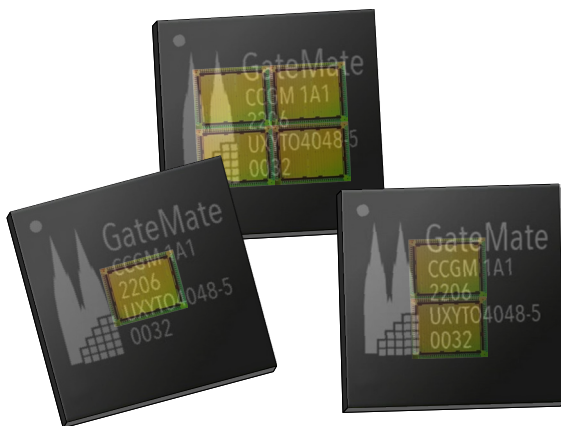


- **Globalfoundries™ 28nm SLP** process (Fab 1 Dresden, Germany)
- **20,480 programmable elements** per FPGA-die
 - 8 inputs or 4+4 inputs + 2 flip-flops
 - 2-bit full adder or 2x2-bit multiplier
- All 162 GPIO configurable as single-ended or LVDS differential pairs with DDR support (**MIPI D-PHY compatible**)
- 32x 40 Kbit RAM cells (Total 1,280 Kbit)
- 4 Clock Generators (PLLs)
- **5 Gbit/s SerDes** Controller
- Temperature range from **-40°C to +125°C**
- Core voltage from 0.9V to 1.1V
I/O voltage from 1.2V to 2.5V (3.3V proven)
- **Open Source Toolchain** using [yosys](#) and [nextpnr](#)
- A1, A2, A4: Patented **Multi-Die** concept



GateMate FPGA Series

Feature Summary by Device



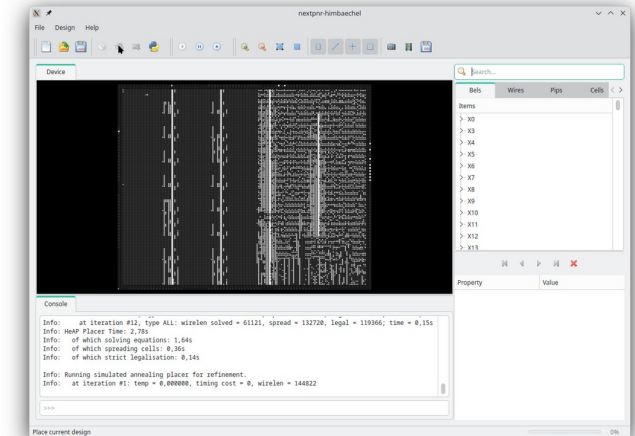
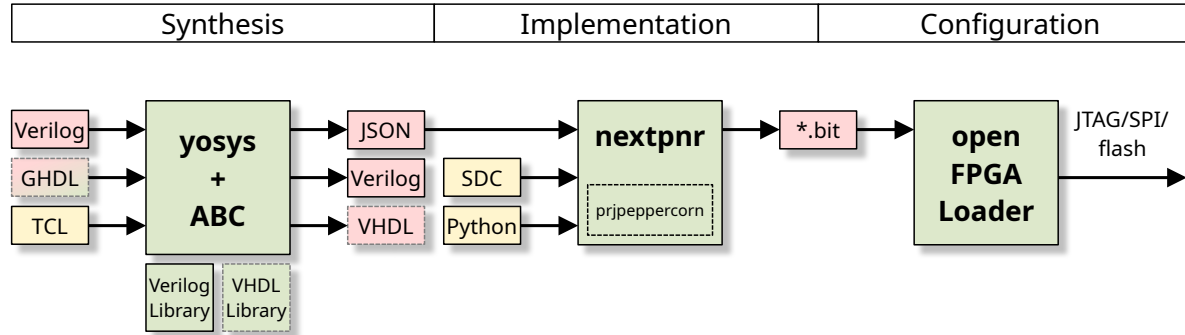
* Patented Technology

Device	CPEs	FFs	Block RAM		PLL	SerDes	GPIO		Package
			20K	40K			Single - ended	Diff. Pairs (LVDS)	
★ A1	20,480	40,960	64	32	4	1	162	81	324 FBGA 15x15 mm
★ A2	40,960	81,920	128	64	8	2	162	81	324 FBGA 15x15 mm
★ A4	81,920	163,840	256	128	16	4	154	77	324 FBGA 15x15 mm
...									
A25	512,000	1,240,000	1600	800	100	25	tba	tba	tba

★ Mass Production ★ Available soon

Toolchain

Open-Source at Every Step



[1] <https://github.com/enjoy-digital/litex>

[2] <https://github.com/YosysHQ/yosys>

[3] <https://github.com/YosysHQ/nextpnr>

[4] <https://github.com/trabucayre/openFPGALoader>

[5] <https://github.com/ghdl/ghdl>

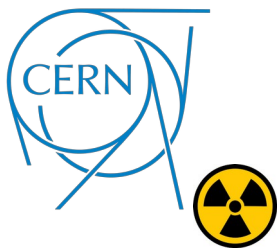
[6] <https://github.com/YosysHQ/prjpeppercorn>

GateMate in Action

What is it capable of?

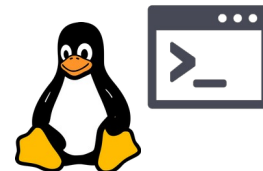


Rad-Hard
Environments
& Space



MIPI Cameras

Boot Linux
with RISC-V
Soft Cores



Open Source Community
& Huge IP Catalogue

High-Speed Serial

The Role of Serializer/Deserializers

Why High-Speed Serial?

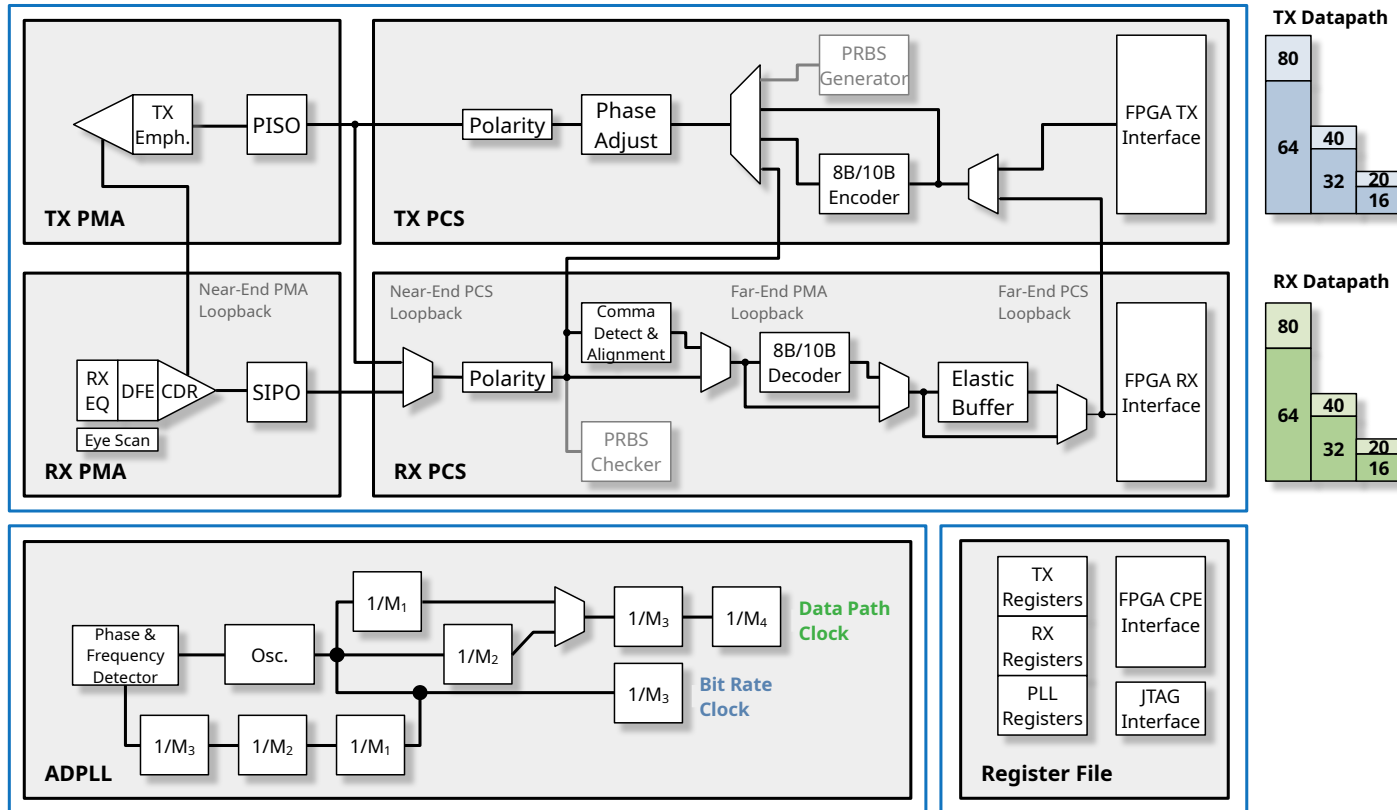
The Role of Serializer/Deserializers



- Bandwidth Demand Outpaces Parallel I/O
 - Parallel buses limited by crosstalk, skew, and physical pin count
 - Difficult to scale beyond a few hundred MHz per line
- High-Speed Serial Advantages
 - Higher Data Rates with fewer pins
 - Lower Power and EMI due to differential signaling and fewer traces
- SerDes: The Enabler
 - Serializer: Converts wide parallel data into high-speed serial stream
 - Deserializer: Recovers original parallel data from serial stream
 - Integrated clock recovery and data alignment logic

Serializer/Deserializer (SerDes)

Full featured, low power consumption



Serializer/Deserializer (SerDes)

ADPLL Settings



$$f_{BRC} = f_{SER_CLK} \cdot \frac{N_1 \cdot N_2 \cdot N_3}{M_3}$$

$$f_{DPC} = f_{SER_CLK} \cdot \frac{N_1 \cdot N_2 \cdot N_3}{M_3} \cdot \frac{1}{M_1 \cdot M_4} = \frac{f_{BRC}}{M_1 \cdot M_4}$$

BRC: Bit Rate Clock

DPC: Data Path Clock

SER_CLK: [100e6, 125e6]

N1: [1, 2]

N2: [2, 3, 4, 5]

N3: [3, 4, 5]

M3: [1, 2, 4]

#	Bitrate Clock [MHz]		Datapath Clock [MHz]		
	100M refclk	125M refclk	80 Bit	40 Bit	20 Bit
1	300	375	3.75	7.50	15.00
2	400	500	5.00	10.00	20.00
3	450	563	5.63	11.25	22.50
4	500	625	6.25	12.50	25.00
5	600	750	7.50	15.00	30.00
6	750	938	9.38	18.75	37.50
7	800	1,000	10.00	20.00	40.00
8	900	1,125	11.25	22.50	45.00
9	1,000	1,250	12.50	25.00	50.00
10	1,200	1,500	15.00	30.00	60.00
11	1,250	1,563	15.63	31.25	62.50
12	1,500	1,875	18.75	37.50	75.00
13	1,600	2,000	20.00	40.00	80.00
14	1,800	2,250	22.50	45.00	90.00
15	2,000	2,500	25.00	50.00	100.00
16	2,400	3,000	30.00	60.00	120.00
17	2,500	3,125	31.25	62.50	125.00
18	3,000	3,750	37.50	75.00	150.00
19	3,200	4,000	40.00	80.00	160.00
20	3,600	4,500	45.00	90.00	180.00
21	4,000	5,000	50.00	100.00	200.00
22	4,800	6,000	60.00	120.00	240.00
23	5,000	6,250	62.50	125.00	250.00
24	6,000	7,500	75.00	150.00	300.00
25	6,400	8,000	80.00	160.00	320.00
26	8,000	10,000	100.00	200.00	400.00
27	10,000	12,500	125.00	250.00	500.00

In Spec. Not in Spec.

5G Serializer/Deserializer (SerDes)

TX Configurable Driver

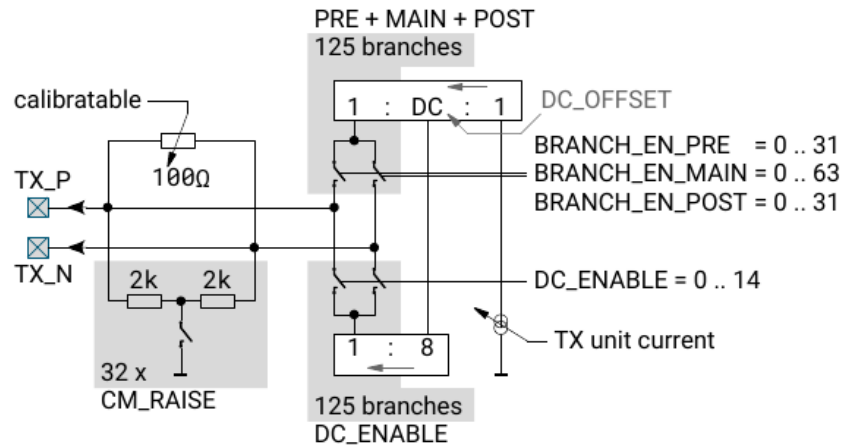


Figure 2.36: Simplified SerDes transmitter driver

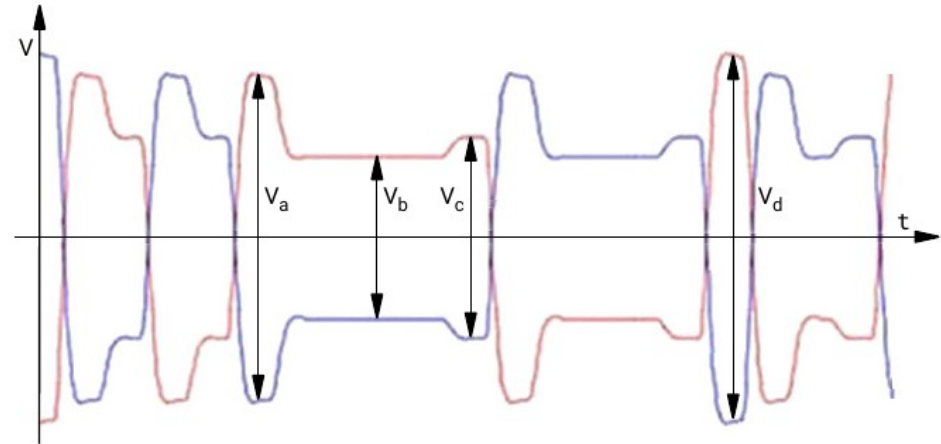


Figure 2.37: Simplified transmitter feed-forward equalization (FFE) scheme for signal (V_a), de-emphasized (V_b), pre-emphasized (V_c) and boost (V_d) voltages

5G Serializer/Deserializer (SerDes)

RX PMA+PCS Features



- 3-tap decision feedback equalizer (DFE)
- Calibratable termination resistor
- Common-mode control
- Electrical idle detector, receiver detection
- Receiver margin analysis with eye measurement
- Clock and data recovery (CDR)
- Comma alignment unit

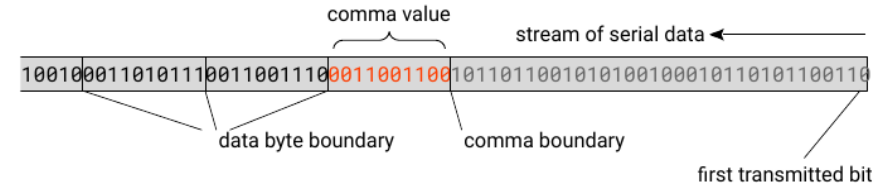


Figure 2.40: Aligning to a 10-bit comma

Alignment	64-Bit Datapath															
	63	56	55	48	47	40	39	32	31	24	23	16	15	8	7	0
32-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit
16-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit
8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit

fields with a gray background indicate the possible positioning of the comma value

SerDes Wizard

Access to the Register File



```
serdes_regfile: python3 — Konsole
New Tab Split View
Copy Paste Find...

FPGA SerDes Parameters (Auto-Update Enabled)

RX_BUF_RESET_TIME 3 RX_CDR_PHASE_ACC_VAL 16800 RX_BUF_BYPASS 0 TX_AMP 20 TX_CM_SAR_RESULT_0 0 PLL_REF_BYPASS 0
RX_PCS_RESET_TIME 3 RX_CDR_FREQ_ACC 0 RX_CLKCOR_USE 0 TX_BRANCH_EN_PRE 25 TX_CM_SAR_RESULT_1 0 PLL_REF_SEL 1
RX_RESET_TIMER_PRESC 0 RX_CDR_PHASE_ACC 0 RX_CLKCOR_MIN_LAT 32 TX_BRANCH_EN_MAIN 30 TX_PMA_RESET_TIME 3 PLL_REF_RTERM 1
RX_RESET_DONE_GATE 0 RX_CDR_SET_ACC_CONFIG 0 RX_CLKCOR_MAX_LAT 39 TX_BRANCH_EN_POST 25 TX_PCS_RESET_TIME 3 PLL_FCNTRL 58
RX_CDR_RESET_TIME 3 RX_CDR_FORCE_LOCK 0 RX_CLKCOR_SEQ_1_0 503 TX_TAIL_CASCODE 4 TX_PCS_RESET_OVR 0 PLL_MAIN_DIVSEL 27
RX_EQA_RESET_TIME 3 RX_ALIGN_MCOMMA_VALUE 643 RX_CLKCOR_SEQ_1_1 503 TX_DC_ENABLE 63 TX_PCS_RESET 0 PLL_OUT_DIVSEL 0
RX_PMA_RESET_TIME 3 RX_MCOMMA_ALIGN_OVR 0 RX_CLKCOR_SEQ_1_2 503 TX_DC_OFFSET 0 TX_PMA_RESET_OVR 0 PLL_CI 0
RX_WAIT_CDR_LOCK 0 RX_MCOMMA_ALIGN 0 RX_CLKCOR_SEQ_1_3 503 TX_CM_RAISE 0 TX_PMA_RESET 0 PLL_CP 80
RX_CALIB_EN 0 RX_ALIGN_PCOMMA_VALUE 380 RX_PMA_LOOPBACK 0 TX_CM_THRESHOLD_0 14 TX_RESET_OVR 0 PLL_A0 0
RX_CALIB_DONE 1 RX_PCOMMA_ALIGN_OVR 0 RX_PCS_LOOPBACK 0 TX_CM_THRESHOLD_1 16 TX_RESET 0 PLL_SCAP 0
RX_CALIB_OVR 0 RX_PCOMMA_ALIGN 0 RX_DATAPATH_SEL 3 TX_SEL_PRE_EI 0 TX_PMA_LOOPBACK 0 PLL_FILTER_SHIFT 2
RX_CALIB_VAL 0 RX_ALIGN_COMMA_WORD 3 RX_PRBS_OVR 0 TX_SEL_POST_EI 0 TX_PCS_LOOPBACK 0 PLL_SAR_LIMIT 2
RX_CALIB_CAL 0 RX_ALIGN_COMMA_ENABLE 1023 RX_PRBS_SEL 0 TX_AMP_EI 15 TX_DATAPATH_SEL 3 PLL_FT 512
RX_RTERM_VCMSEL 4 RX_SLIDE_MODE 0 RX_LOOPBACK_OVR 0 TX_BRANCH_EN_PRE_EI 0 TX_PRBS_OVR 0 PLL_OPEN_LOOP 0
RX_RTERM_PD 0 RX_COMMA_DETECT_EN_OVR 0 RX_PRBS_CNT_RESET 0 TX_BRANCH_EN_MAIN_EI 63 TX_PRBS_SEL 0 PLL_SCAP_AUTO_CAL 1
RX_EQA_CKP_LF 163 RX_COMMA_DETECT_EN 0 RX_POWER_DOWN_OVR 0 TX_BRANCH_EN_POST_EI 0 TX_PRBS_FORCE_ERR 0 PLL_LOCKED 1
RX_EQA_CKP_HF 163 RX_SLIDE[0] 0 RX_POWER_DOWN_N 1 TX_TAIL_CASCODE_EI 4 TX_LOOPBACK_OVR 0 PLL_CAP_FT_OF 0
RX_EQA_CKP_OFFSET 1 RX_SLIDE[1] 0 RX_PRESENT 0 TX_DC_ENABLE_EI 63 TX_POWER_DOWN_OVR 0 PLL_CAP_FT_UP 0
RX_EN_EQA 0 RX_EYE_MEAS_EN 0 RX_DETECT_DONE 0 TX_DC_OFFSET_EI 0 TX_POWER_DOWN_N 1 PLL_CAP_FT 380
RX_EQA_LOCK_CFG 0 RX_EYE_MEAS_CFG 0 RX_BUF_ERR 0 TX_CM_RAISE_EI 0 TX_ELEC_IDLE_OVR 0 PLL_CAP_STATE 2
RX_EQA_LOCKED 0 RX_MON_PH_OFFSET 0 RX_RESET_OVR 0 TX_CM_THRESHOLD_0_EI 14 TX_ELEC_IDLE 0 PLL_SYNC_VALUE 0
RX_TH_MON1 8 RX_EYE_MEAS_CORRECT_115 0 RX_RESET 0 TX_CM_THRESHOLD_1_EI 16 TX_DETECT_RX_OVR 0 PLL_BISC_MODE 5
RX_EN_EQA_EXT_VALUE[0] 0 RX_EYE_MEAS_WRONG_115 0 RX_PMA_RESET_OVR 0 TX_SEL_PRE_RXDET 0 TX_DETECT_RX 0 PLL_BISC_TIMER_MAX 12
RX_TH_MON2 8 RX_EYE_MEAS_CORRECT_005 0 RX_PMA_RESET 0 TX_SEL_POST_RXDET 0 TX_POLARITY_OVR 0 PLL_BISC_OPT_DET_IND 0
RX_EN_EQA_EXT_VALUE[1] 0 RX_EYE_MEAS_WRONG_005 0 RX_EQA_RESET_OVR 0 TX_AMP_RXDET 15 TX_POLARITY 0 PLL_BISC_PFD_SEL 0
RX_TAPW 8 RX_EYE_MEAS_CORRECT_0015 0 RX_EQA_RESET 0 TX_BRANCH_EN_PRE_RXDET 0 TX_BB10B_EN_OVR 0 PLL_BISC_DLY_DIR 0
RX_EN_EQA_EXT_VALUE[2] 0 RX_EYE_MEAS_WRONG_0015 0 RX_CDR_RESET_OVR 0 TX_BRANCH_EN_MAIN_RXDET 63 TX_BB10B_EN 0 PLL_BISC_COR_DLY 1
RX_AFE_OFFSET 8 RX_EYE_MEAS_CORRECT_1105 0 RX_CDR_RESET 0 TX_BRANCH_EN_POST_RXDET 0 TX_DATA_OVR 0 PLL_BISC_CAL_SIGN 1
RX_EN_EQA_EXT_VALUE[3] 0 RX_EYE_MEAS_WRONG_1105 0 RX_PCS_RESET_OVR 0 TX_TAIL_CASCODE_RXDET 4 TX_DATA_CNT 4 PLL_BISC_CAL_AUTO 1
RX_EQA_TAPW 0 RX_EI_BIAS 4 RX_PCS_RESET 0 TX_DC_ENABLE_RXDET 63 TX_DATA_VALID 0 PLL_BISC_CP_MIN 6
RX_TH_MON 15 RX_BUF_SEL 4 RX_BUF_RESET_OVR 0 TX_DC_OFFSET_RXDET 0 TX_BUF_ERR 0 PLL_BISC_CP_MAX 30
RX_OFFSET 8 RX_EN_EI_DETECTOR_OVR 0 RX_BUF_RESET 0 TX_CM_RAISE_RXDET 0 TX_RESET_DONE 1 PLL_BISC_CP_START 6
RX_EQA_CONFIG 448 RX_EN_EI_DETECTOR 0 RX_POLARITY_OVR 0 TX_CM_THRESHOLD_0_RXDET 14 TX_DATA 0 PLL_BISC_DLY_PFD_MON_REF 0
RX_AFE_PEAK 15 RX_EI_EN 0 RX_POLARITY 0 TX_CM_THRESHOLD_1_RXDET 16 PLL_EN_ADPLL_CTRL 1 PLL_BISC_DLY_PFD_MON_DIV 2
RX_AFE_GAIN 8 RX_PRBS_ERR_CNT 0 RX_BB10B_EN_OVR 0 TX_CALIB_EN 0 PLL_CONFIG_SEL 1 PLL_BISC_TIMER_DONE 0
RX_AFE_VCMSEL 4 RX_PRBS_LOCKED 0 RX_BB10B_EN 0 TX_CALIB_DONE 1 PLL_SET_OP_LOCK 0 PLL_BISC_CP 48
RX_CDR_CKP 248 RX_DATA_SEL 0 RX_BB10B_BYPASS 0 TX_CALIB_OVR 0 PLL_ENFORCE_LOCK 0 PLL_BISC_CO 63582
RX_CDR_CKT 0 RX_DATA[15:0] 11196 RX_BB10B_REALIGN 1 TX_CALIB_VAL 0 PLL_DISABLE_LOCK 0 SERDES_ENABLE 0
RX_CDR_TRANS_TH 128 RX_DATA[31:16] 33809 RX_BYTE_REALIGN 1 TX_CALIB_CAL 0 PLL_LOCK_WINDOW 1 SERDES_AUTO_INIT 0
RX_CDR_LOCK_CFG 11 RX_DATA[47:32] 18962 RX_RESET_DONE 1 TX_CM_REG_KI 128 PLL_FAST_LOCK 1 SERDES_TESTMODE 1
RX_CDR_LOCKED 1 RX_DATA[63:48] 41256 TX_SEL_PRE 0 TX_CM_SAR_EN 0 PLL_SYNC_BYPASS 0
RX_CDR_FREQ_ACC_VAL 0 RX_DATA[79:64] 4740 TX_SEL_POST 0 TX_CM_REG_EN 1 PLL_PFD_SELECT 0

Bit Rate Clock: 5000.00 MHz
TX Data Path Clock: 62.50 MHz

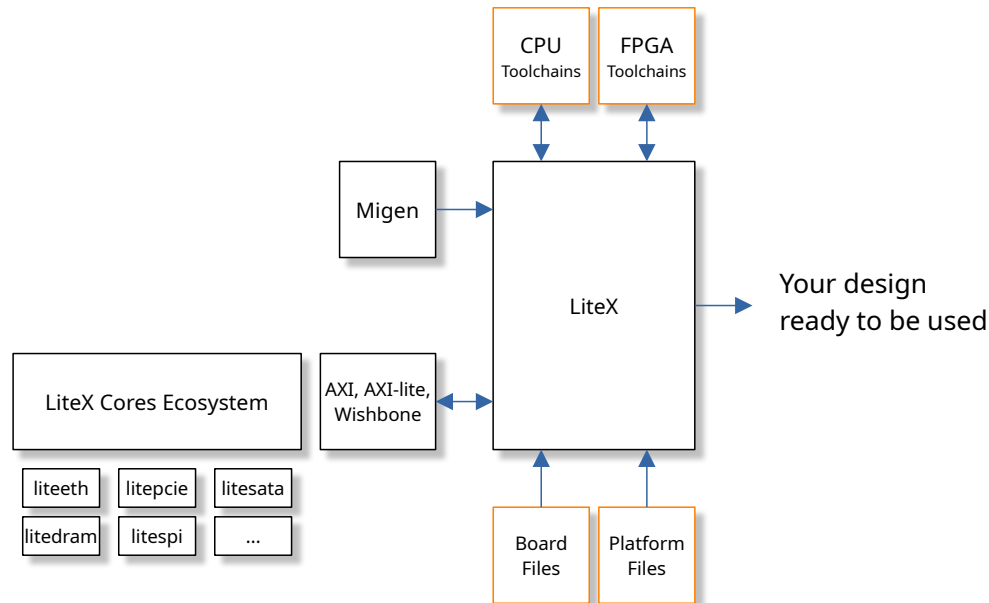
[Arrow Keys] Navigate | [Enter] Edit | [/] Find | [h] Toggle HEX/DEC | [q] Quit
```

GateMate SerDes in Action

And why it is so easy to use

Massive IP Catalogue: LiteX

„Build your hardware, easily!“



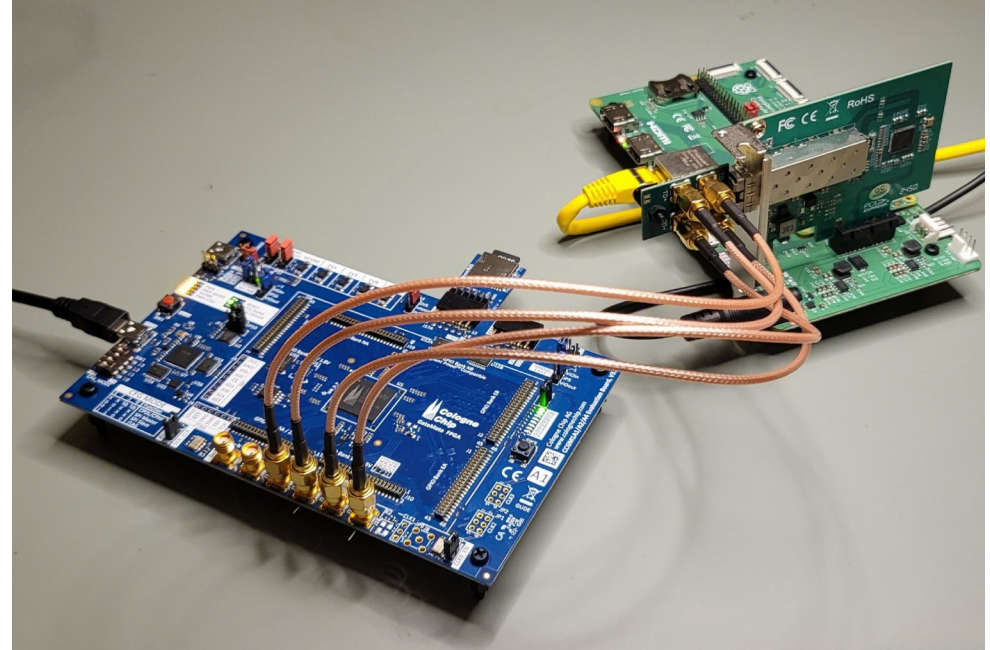
Name	Build Status	Description
LiteX-Boards	ci passing	Boards support
LiteDRAM	ci passing	DRAM
LiteEth	ci passing	Ethernet
LitePCIe	ci passing	PCIe
LiteSATA	ci passing	SATA
LiteSDCard	ci passing	SD card
LiteICLink	ci passing	Inter-Chip communication
LiteJESD204B	ci passing	JESD204B
LiteSPI	ci passing	SPI/SPI-Flash
LiteScope	ci passing	Logic analyzer

[1] <https://github.com/enjoy-digital/litex>

1000BASE-X Implementation

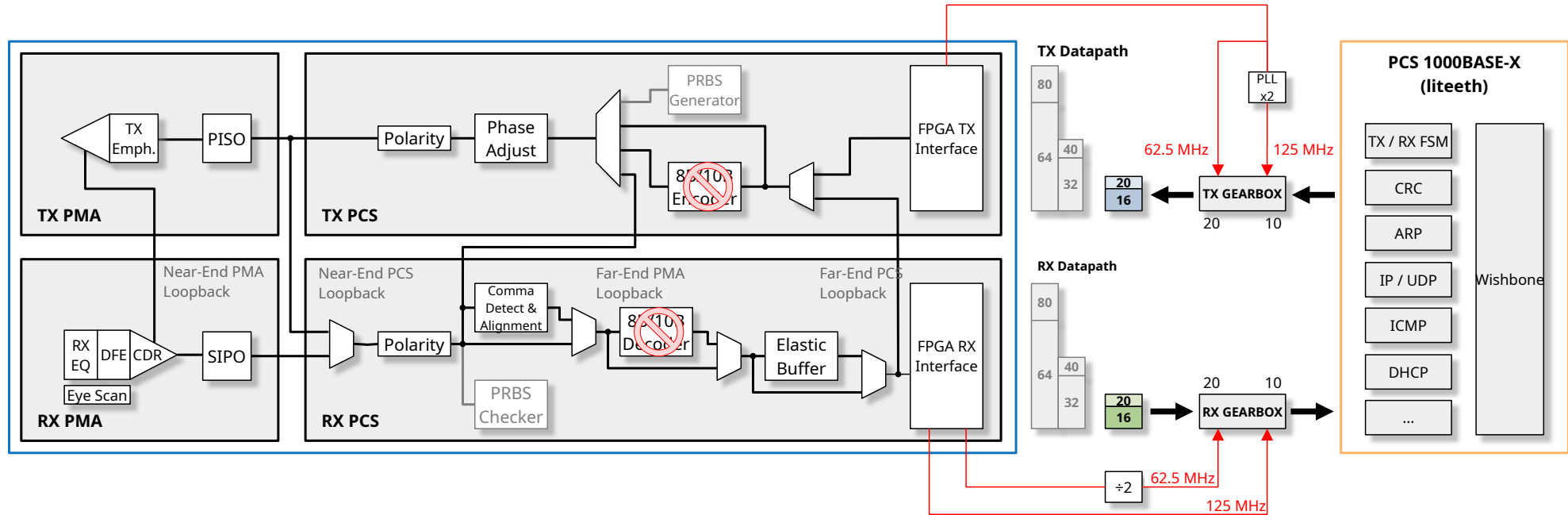
Liteeth Implementation

- Build on top of Lites' **PCS-1000BASE-X**
- SerDes PCS: bypassed (see next slide)
- Uses 20/16-bit datapath
- Requires TX+RX gearboxes for 10-bit datapath
- Fabric speed: 125 MHz



1000BASE-X Implementation

Liteeth Implementation

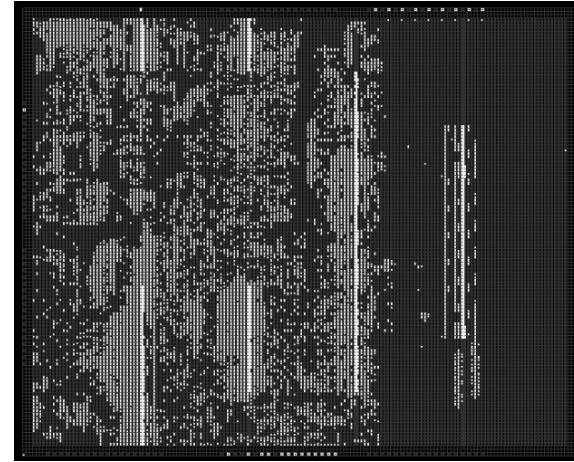


[1] <https://github.com/enjoy-digital/liteeth/tree/master/liteeth/phy>

1000BASE-X Implementation

Resource Utilization

- Configuration:
 - VexRiscv (RV32I)
 - HyperRAM memory controller
 - UART interface
 - ROM (for bootloader)
 - 1000BASE-X PCS + MAC
- Processing time: **1m 18s**
(litex + gcc + yosys + nextpnr)



```
Info: Device utilisation:
Info:      USR_RSTN:      1/      1    100%
Info:      GPIO:         25/     162    15%
Info:      CLKIN:          1/      1    100%
Info:      GLBOUT:         1/      1    100%
Info:      PLL:            2/      4     50%
Info:      CFG_CTRL:       0/      1     0%
Info:      RAM:           17/     32    53%
Info:      SERDES:         1/      1    100%
Info:      CPE_HALF:    12764/   40960    31%
```

GateMate SerDes Demo

Contact

Patrick Urban, M.Sc.

Cologne Chip AG

Eintrachtstr. 113

50668 Köln

<https://colognechip.com>

patrick.urban@colognechip.com



Add me on LinkedIn!

