GateMate™ FPGA

High-Speed Transceiver (SerDes)

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FPGA Conference Europe

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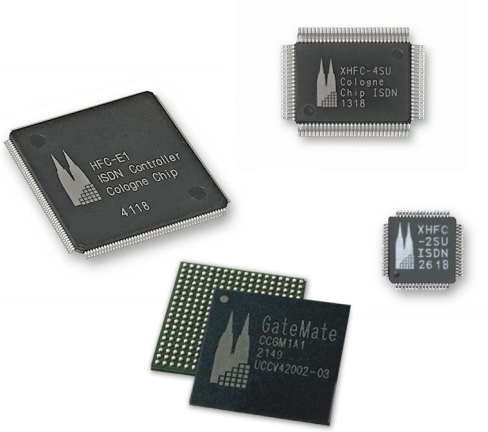
Agenda

1. Introduction to GateMate FPGA
   - Architecture & Toolchain
2. Detailled look into the GateMate SerDes
   - Features & Tools
3. 1000BASE-X Implementation & Example
   - SerDes Wizard & Loopback Example

Company Overview

1994	Founding year of **Cologne Chip Designs GmbH**.
1996	Presentation of world's first single-chip-solution for ISDN.
2000	Rebranding to **Cologne Chip AG** and sales in millions of units after annual growth rates by 100%
2007	Establishment of the **XHFC-Series** with open access to drivers and software; part of Linux Kernel since v. 2.6.27.
2020	Introduction of a new product line: **GateMate FPGA**.



> 30 Years

Experience in Semiconductor Business

Certified Quality

100 %

Always on-time Same-Day Deliveries

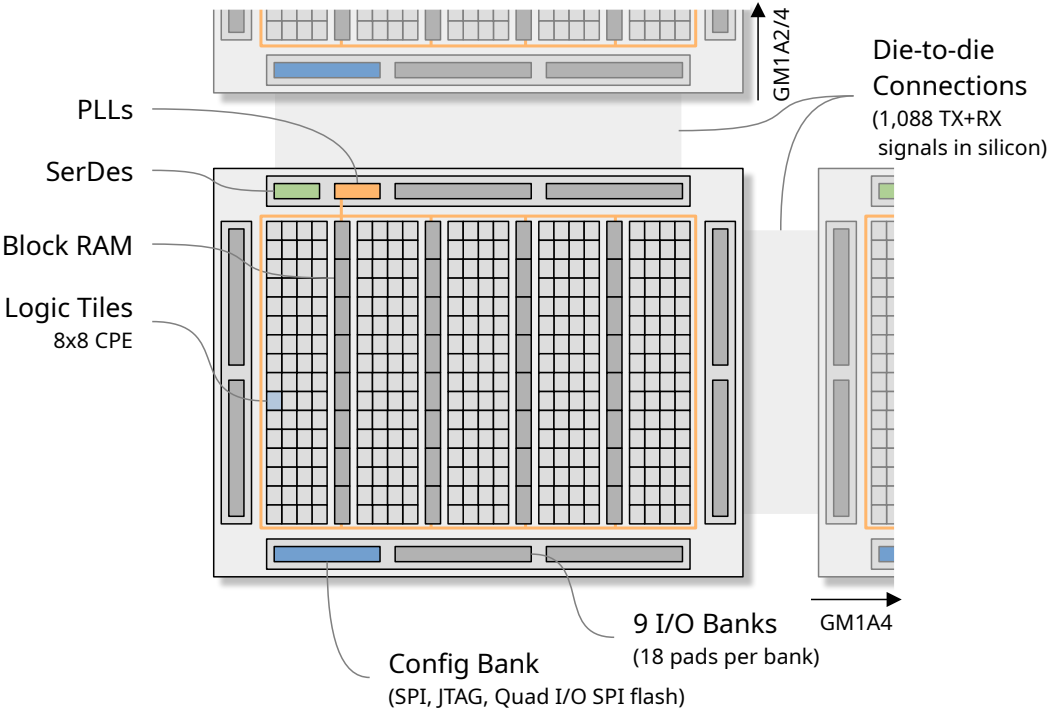
designed and manufactured in Germany

Reliable Supply Chain

GateMate FPGA

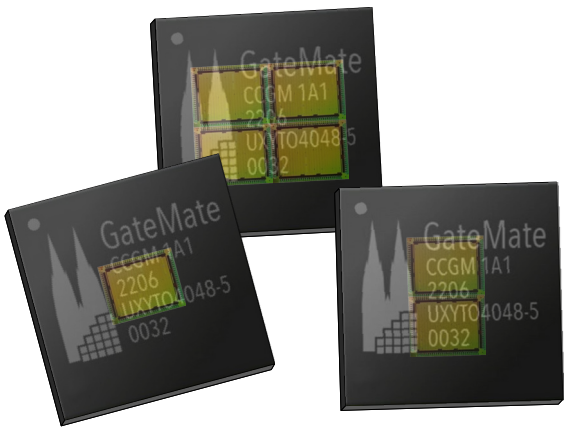
Features at a glance

- **Globalfoundries™ 28nm SLP** process (Fab 1 Dresden, Germany)
- **20,480 programmable elements** per FPGA-die
  - 8 inputs or 4+4 inputs + 2 flip-flops
  - 2-bit full adder or 2x2-bit multiplier
- All 162 GPIO configurable as single-ended or LVDS differential pairs with DDR support (**MIPI D-PHY compatible**)
- 32x 40 Kbit RAM cells (Total 1,280 Kbit)
- 4 Clock Generators (PLLs)
- **5 Gbit/s SerDes** Controller
- Temperature range from **-40°C to +125°C**
- Core voltage from 0.9V to 1.1V
  I/O voltage from 1.2V to 2.5V (3.3V proven)
- **Open Source Toolchain** using yosys and nextpnr
- A1, A2, A4: Patented Multi-Die concept



GateMate FPGA Series

Feature Summary by Device



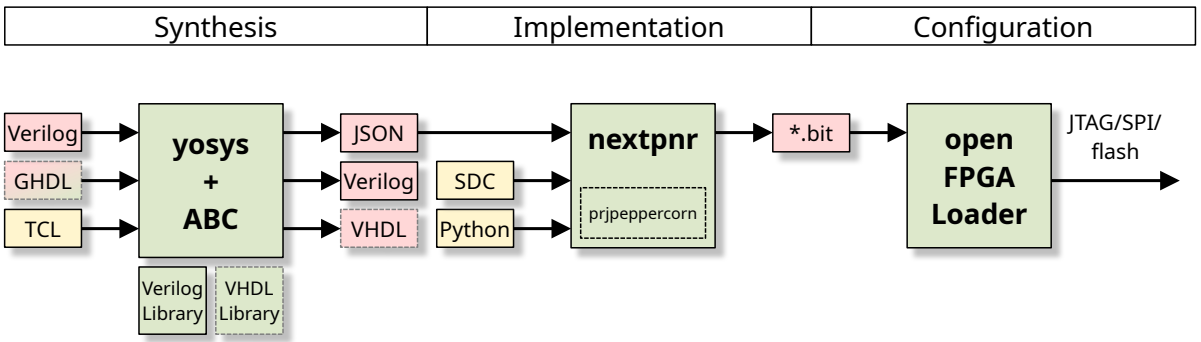
* Patented Technology

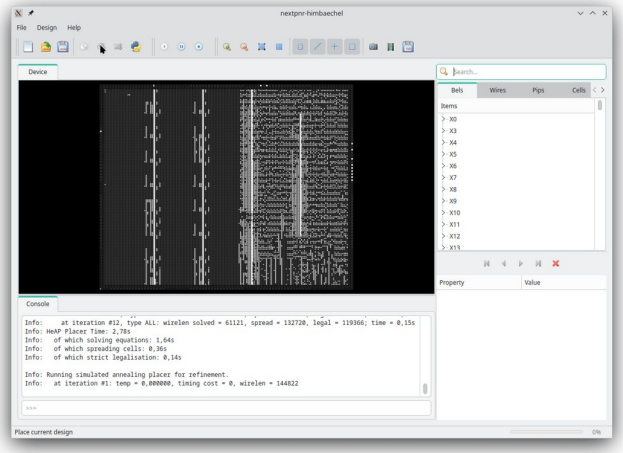
Device	CPEs	FFs	Block RAM		PLL	SerDes	GPIO		Package
			20K	40K			Single-ended	Diff. Pairs (LVDS)	
★ **A1**	20,480	40,960	64	32	4	1	162	81	324 FBGA 15x15 mm
★ **A2**	40,960	81,920	128	64	8	2	162	81	324 FBGA 15x15 mm
★ **A4**	81,920	163,840	256	128	16	4	154	77	324 FBGA 15x15 mm
...									
A25	512,000	1,240,000	1600	800	100	25	tba	tba	tba

★ Mass Production ★ Avaliable soon

Toolchain

Open-Source at Every Step





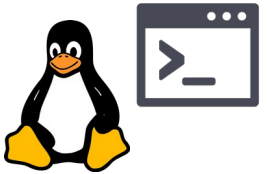
[1] https://github.com/enjoy-digital/litex
[2] https://github.com/YosysHQ/yosys
[3] https://github.com/YosysHQ/nextpnr
[4] https://github.com/trabucayre/openFPGALoader
[5] https://github.com/ghdl/ghdl
[6] https://github.com/YosysHQ/prjpeppercorn

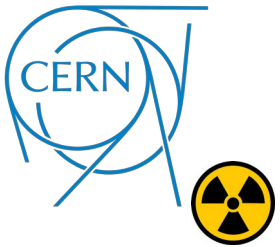
GateMate in Action

What is it capable of?

Rad-Hard
Envionments
& Space

Boot Linux
with RISC-V
Soft Cores





MIPI Cameras

Open Source Community
& Huge IP Catalogue

High-Speed Serial

The Role of Serializer/Deserializers

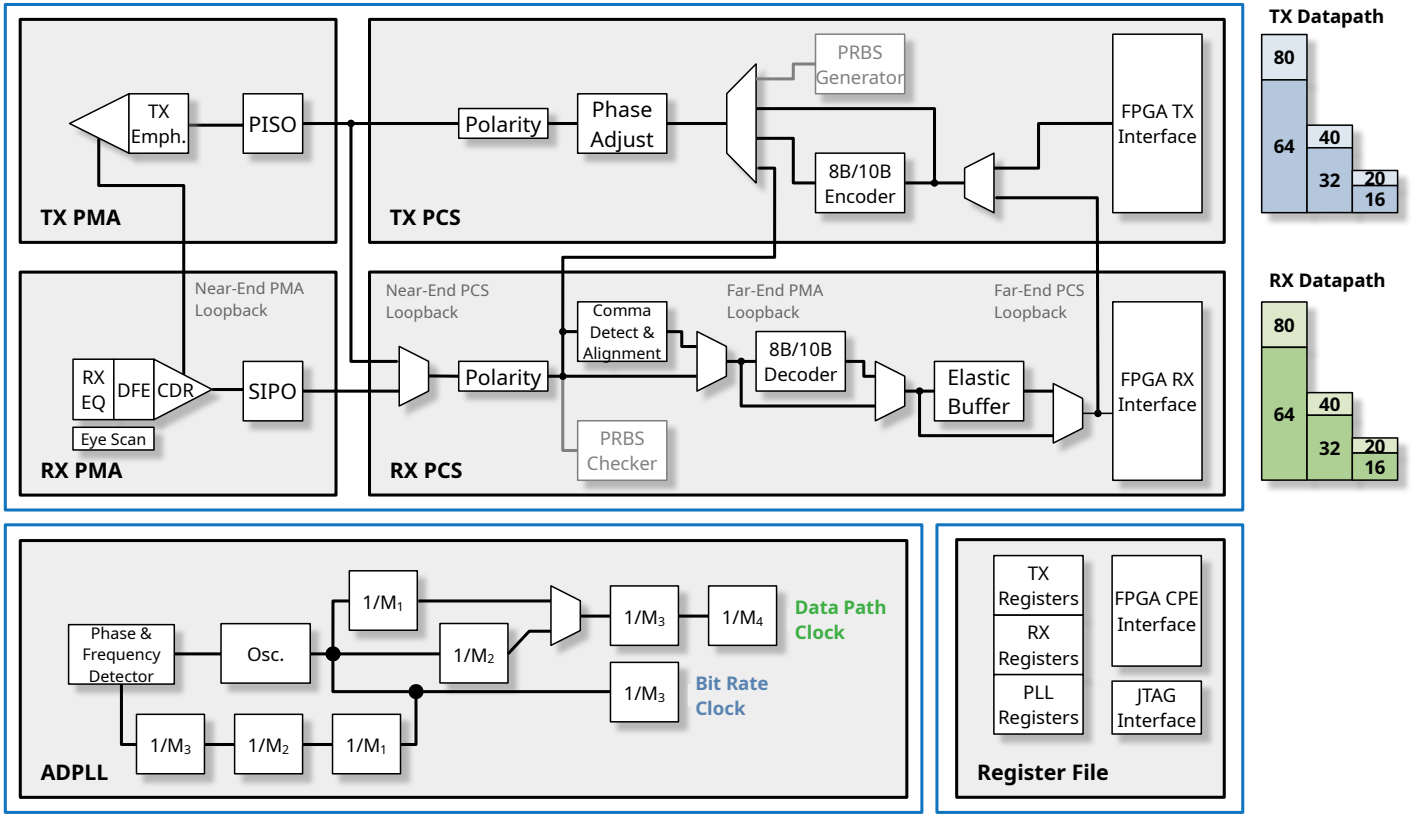
Why High-Speed Serial?

The Role of Serializer/Deserializers

- Bandwidth Demand Outpaces Parallel I/O
  - Parallel buses limited by crosstalk, skew, and physical pin count
  - Difficult to scale beyond a few hundred MHz per line
- High-Speed Serial Advantages
  - Higher Data Rates with fewer pins
  - Lower Power and EMI due to differential signaling and fewer traces
- SerDes: The Enabler
  - Serializer: Converts wide parallel data into high-speed serial stream
  - Deserializer: Recovers original parallel data from serial stream
  - Integrated clock recovery and data alignment logic

Serializer/Deserializer (SerDes)

Full featured, low power consumption



Serializer/Deserializer (SerDes)

ADPLL Settings

$$f_{BRC} = f_{SER\_CLK} \cdot \frac{N_1 \cdot N_2 \cdot N_3}{M_3}$$

$$f_{DPC} = f_{SER\_CLK} \cdot \frac{N_1 \cdot N_2 \cdot N_3}{M_3} \cdot \frac{1}{M_1 \cdot M_4} = \frac{f_{BRC}}{M_1 \cdot M_4}$$

BRC: Bit Rate Clock
DPC: Data Path Clock

SER_CLK: [100e6, 125e6]
N1: [1, 2]
N2: [2, 3, 4, 5]
N3: [3, 4, 5]
M3: [1, 2, 4]

	Bitrate Clock [MHz]		Datapath Clock [MHz]		
#	100M refclk	125M refclk	80 Bit	40 Bit	20 Bit
1	300	375	3.75	7.50	15.00
2	400	500	5.00	10.00	20.00
3	450	563	5.63	11.25	22.50
4	500	625	6.25	12.50	25.00
5	600	750	7.50	15.00	30.00
6	750	938	9.38	18.75	37.50
7	800	1,000	10.00	20.00	40.00
8	900	1,125	11.25	22.50	45.00
9	1,000	1,250	12.50	25.00	50.00
10	1,200	1,500	15.00	30.00	60.00
11	1,250	1,563	15.63	31.25	62.50
12	1,500	1,875	18.75	37.50	75.00
13	1,600	2,000	20.00	40.00	80.00
14	1,800	2,250	22.50	45.00	90.00
15	2,000	2,500	25.00	50.00	100.00
16	2,400	3,000	30.00	60.00	120.00
17	2,500	3,125	31.25	62.50	125.00
18	3,000	3,750	37.50	75.00	150.00
19	3,200	4,000	40.00	80.00	160.00
20	3,600	4,500	45.00	90.00	180.00
21	4,000	5,000	50.00	100.00	200.00
22	4,800	6,000	60.00	120.00	240.00
23	5,000	6,250	62.50	125.00	250.00
24	6,000	7,500	75.00	150.00	300.00
25	6,400	8,000	80.00	160.00	320.00
26	8,000	10,000	100.00	200.00	400.00
27	10,000	12,500	125.00	250.00	500.00

In Spec. Not in Spec.

5G Serializer/Deserializer (SerDes)

TX Configurable Driver

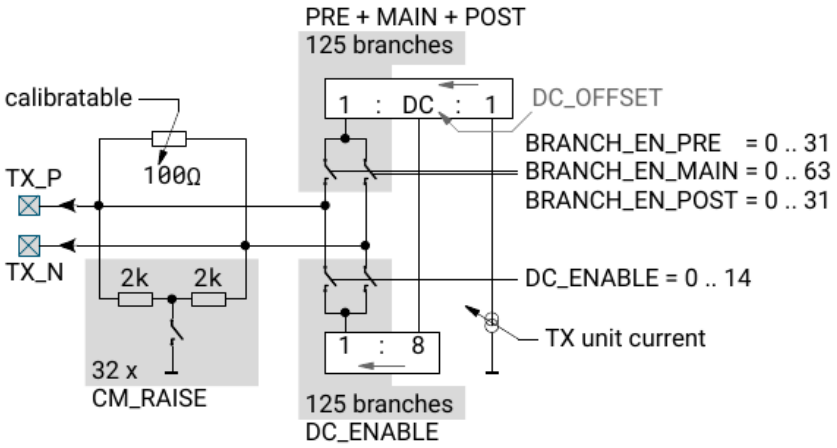


Figure 2.36: *Simplified SerDes transmitter driver*

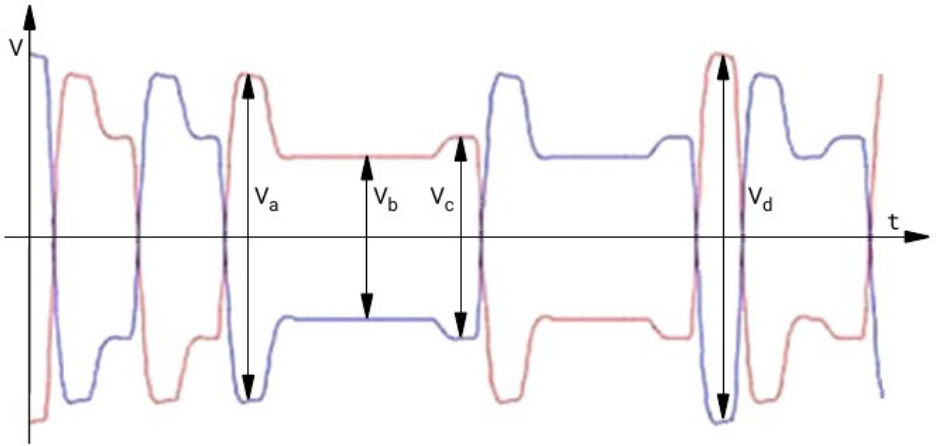


Figure 2.37: *Simplified transmitter feed-forward equalization (FFE) scheme for signal (V_a), de-emphasized (V_b), pre-emphasized (V_c) and boost (V_d) voltages*

5G Serializer/Deserializer (SerDes)

RX PMA+PCS Features

- 3-tap decision feedback equalizer (DFE)
- Calibratable termination resistor
- Common-mode control
- Electrical idle detector, receiver detection
- Receiver margin analysis with eye measurement
- Clock and data recovery (CDR)
- Comma alignment unit

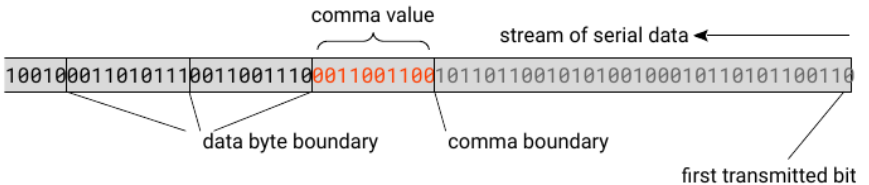


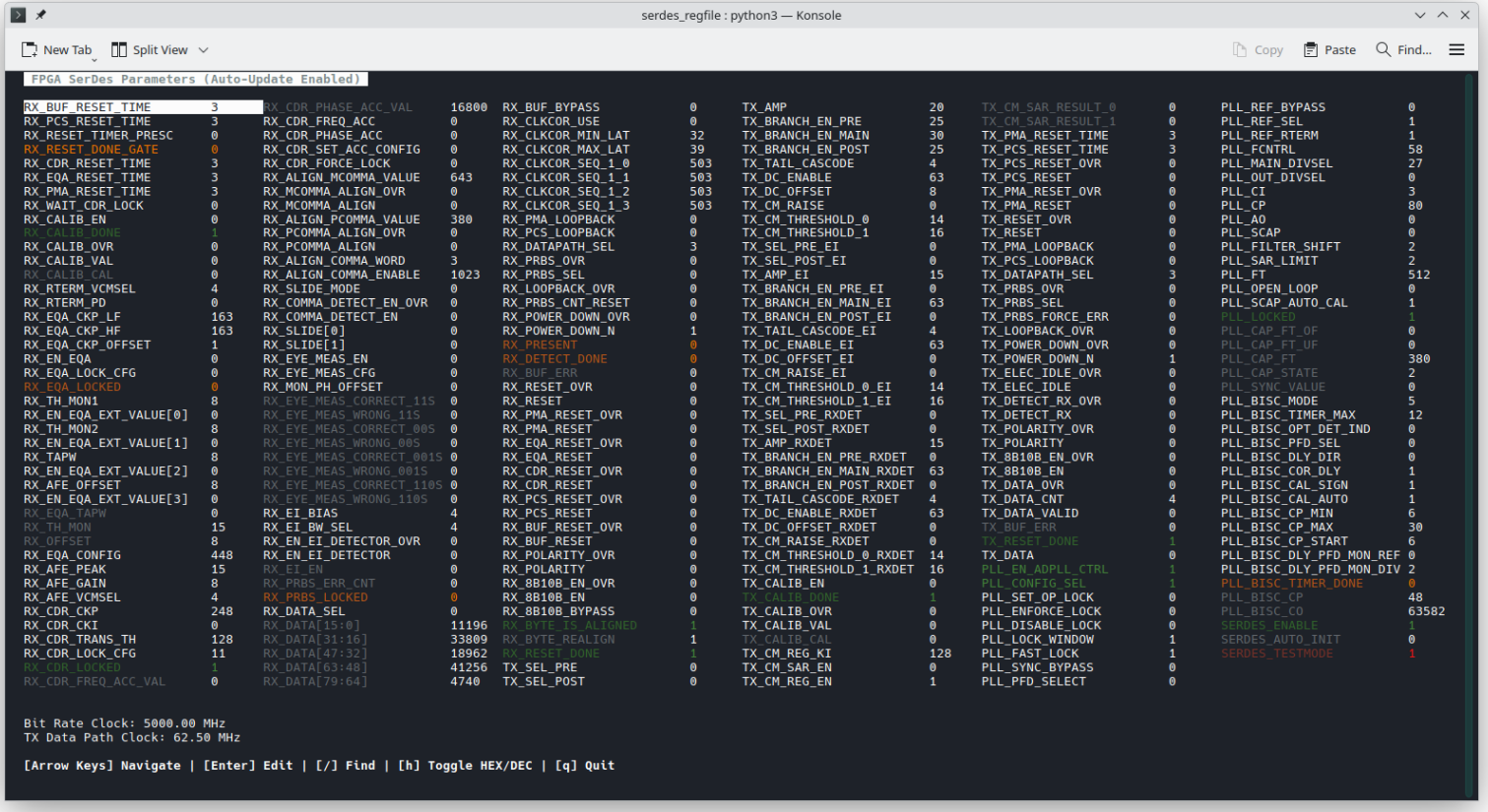
Figure 2.40: *Aligning to a 10-bit comma*

Alignment	64-Bit Datapath							
	63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0
32-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit
16-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit
8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit	8-Bit

fields with a gray background indicate the possible positioning of the comma value

SerDes Wizard

Access to the Register File

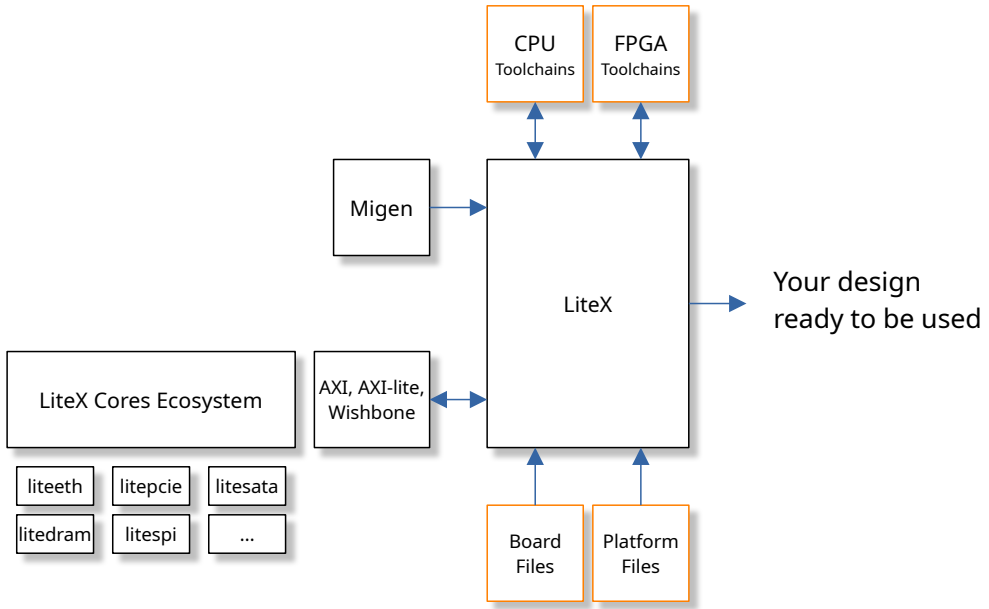


GateMate SerDes in Action

And why it is so easy to use

Massive IP Catalogue: LiteX

„Build your hardware, easily!“



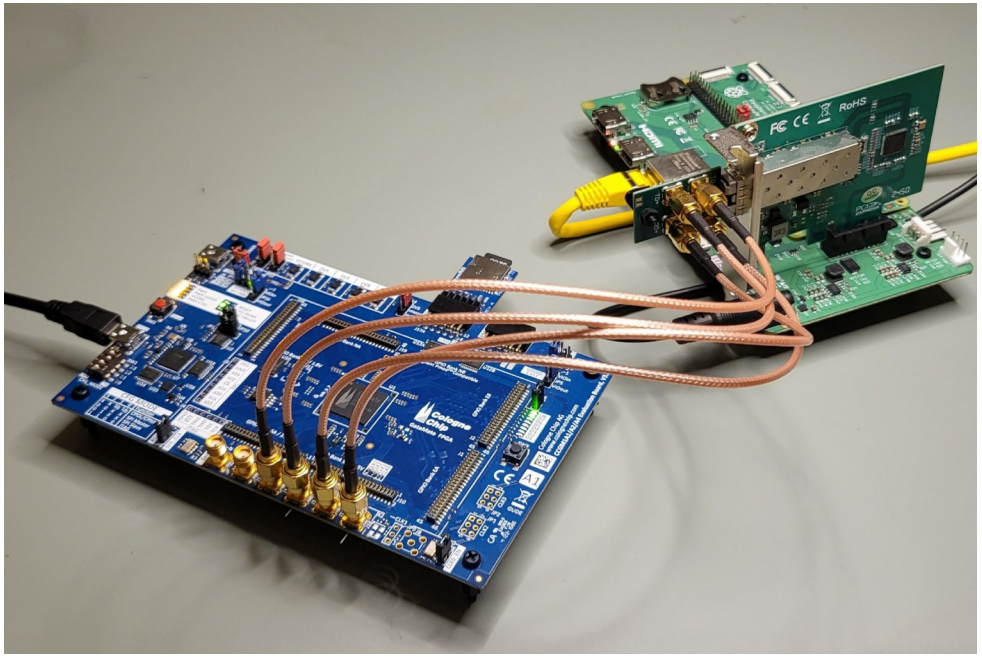
Name	Build Status	Description
LiteX-Boards	ci passing	Boards support
LiteDRAM	ci passing	DRAM
LiteEth	ci passing	Ethernet
LitePCIe	ci passing	PCIe
LiteSATA	ci passing	SATA
LiteSDCard	ci passing	SD card
LiteICLink	ci passing	Inter-Chip communication
LiteJESD204B	ci passing	JESD204B
LiteSPI	ci passing	SPI/SPI-Flash
LiteScope	ci passing	Logic analyzer

[1] https://github.com/enjoy-digital/litex

1000BASE-X Implementation

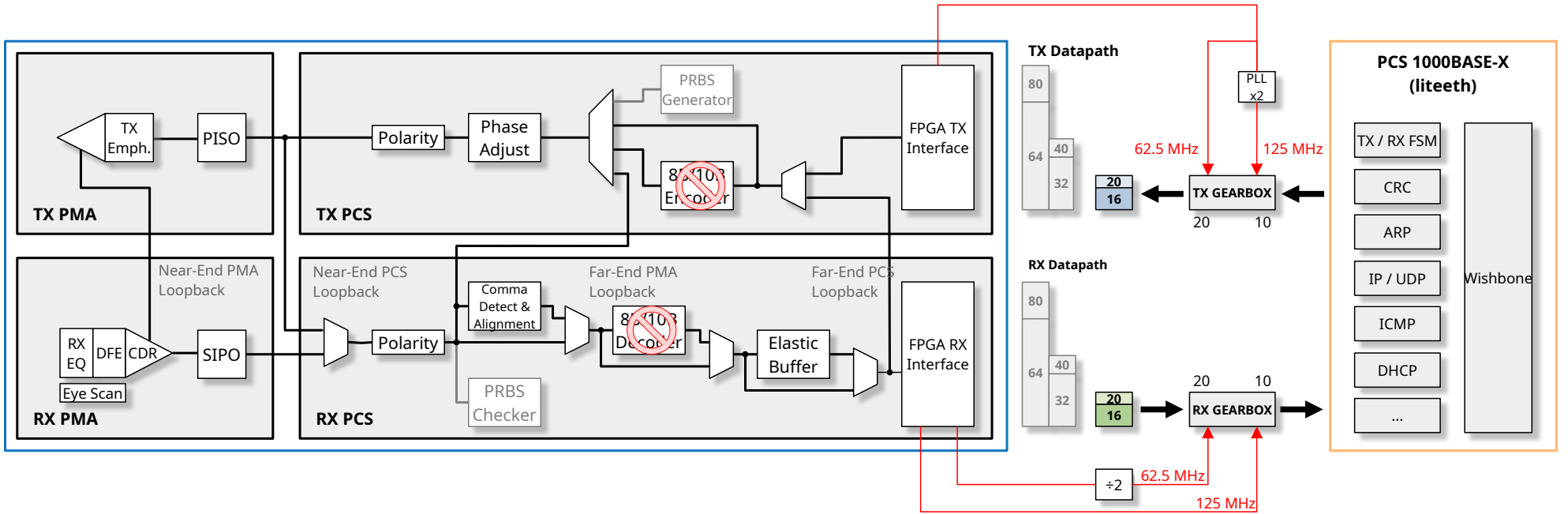
Liteeth Implementation

- Build on top of Litex' PCS-1000BASE-X
- SerDes PCS: bypassed
  (see next slide)
- Uses 20/16-bit datapath
- Requires TX+RX gearboxes for 10-bit datapath
- Fabric speed: 125 MHz



1000BASE-X Implementation

Liteeth Implementation

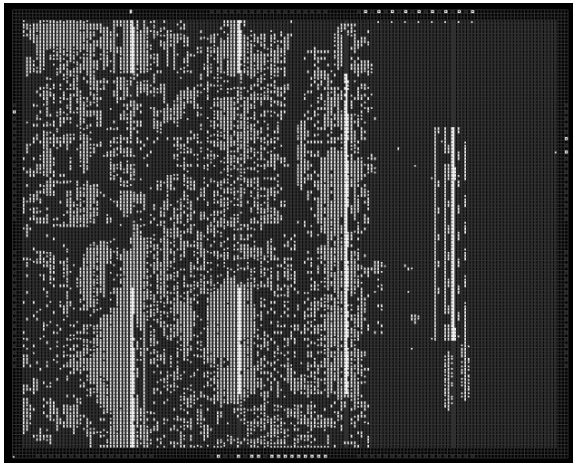


[1] https://github.com/enjoy-digital/liteeth/tree/master/liteeth/phy

1000BASE-X Implementation

Resource Utilization

- Configuration:
  - VexRiscv (RV32I)
  - HyperRAM memory controller
  - UART interface
  - ROM (for bootloader)
  - 1000BASE-X PCS + MAC
- Processing time: 1m 18s
  (litex + gcc + yosys + nextpnr)



```
Info: Device utilisation:
Info:              USR_RSTN:      1/      1   100%
Info:                  GPIO:     25/    162    15%
Info:                 CLKIN:      1/      1   100%
Info:                GLBOUT:      1/      1   100%
Info:                   PLL:      2/      4    50%
Info:              CFG_CTRL:      0/      1     0%
Info:                   RAM:     17/     32    53%
Info:                SERDES:      1/      1   100%
Info:              CPE_HALF:  12764/  40960    31%
```

GateMate SerDes Demo

Contact

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