GateMate™ FPGA User Guide

Interface Guide for Peripheral Devices with 3.3 V Signaling

UG1003

User Guide December 2023

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About this Document

This User Guide covers the interfacing of the Cologne Chip GateMate™ FPGA Series to peripheral devices with 3.3 V signaling and is part of the GateMate™ documentation collection.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA
- **DS1001** – GateMate™ FPGA CCGM1A1 Datasheet
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Cologne Chip provides a comprehensive technical support. Please visit our website for more information or contact our support team.

1 Introduction

This document describes how GateMate™ FPGAs can be connected to peripheral devices with 3.3 V signaling.

GateMate's GPIO supply voltage VDDIO is not allowed to exceed 2.7 V. Input voltages of 3.3 V or higher are not supported from the GateMate FPGA on chip level.

This is due to the fact that GateMate devices also support 1.2 V interface standards (e.g. JESD8-26). From the chip technology it is hard to achieve reasonable performance at both 1.2 V and 3.3 V interface levels.

Any voltage above VDDIO supply voltage should be avoided on the GateMate pins.

2 Unidirectional Interfacing

2.1 GateMate Output to Peripheral Input

In cases where 2.5 V is used as GateMate VDDIO voltage and the peripheral receiver is an LVCMOS input with 3.3 V signaling, no interface circuitry is needed as shown in Figure 1.

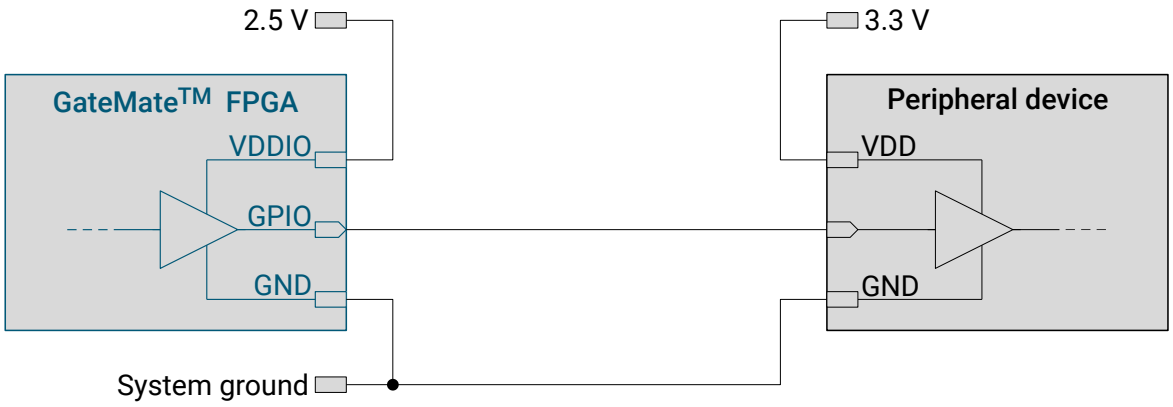

Figure 1: *GateMate output interfacing*

2.2 GateMate Input from Peripheral Output

If the peripheral driver connected to a GateMate input pin is driving 3.3 V and GateMate VDDIO voltage is 2.5 V, an interface circuitry is needed.

2.2.1 Simple Interface for Low Speed Signals

For low speed signals a simple series resistor is sufficient as shown in Figure 2. The input overvoltage security circuitry of the GateMate input pin will limit the input voltage.

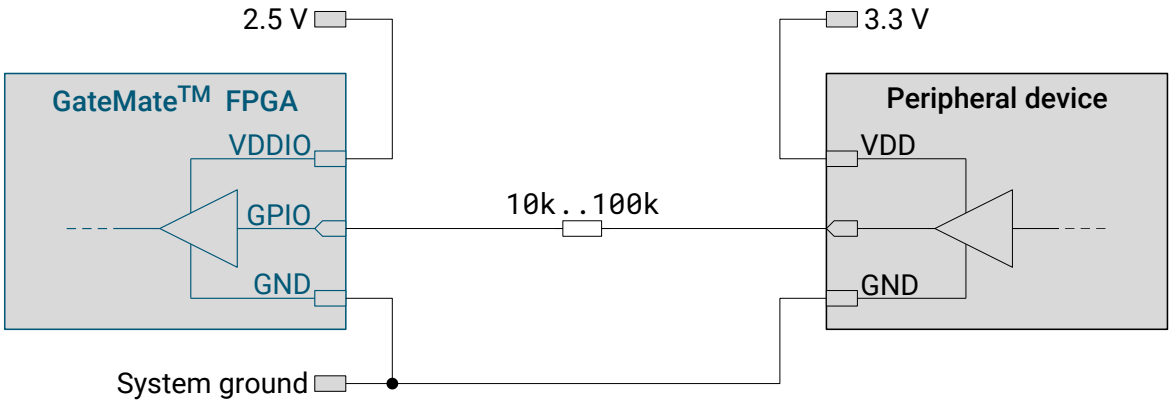

Figure 2: *Low speed GateMate input interfacing*

2.2.2 Interfacing for High Speed Signals

For high speed signal transmission an active interface circuit is recommended. The solution shown in Figure 3 has a delay of less than 10 ns and is therefore also suitable for high speed communication. The 74LV245 or 74LVC245 are 5 V tolerant devices that can be used with 2.5 V supply voltage and are able to have an input voltage of up to 5 V.

> **Please note!**
>
> Please make sure that you use an overvoltage-tolerant device, as the characteristics of the devices from various chip manufacturers may differ.

Hint: Figure 3 may also be an alternative to Figure 2 for low-speed signal buses in order to reduce the assembly costs of the PCB.

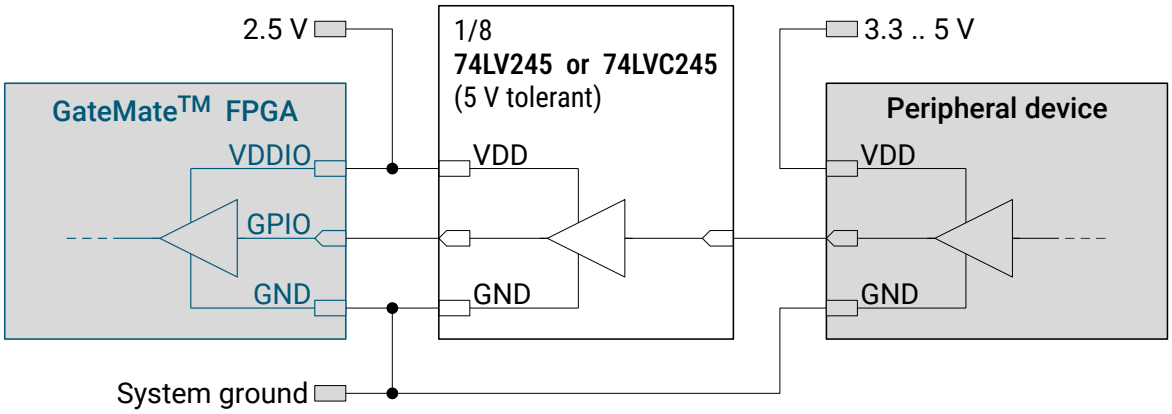

Figure 3: *High speed GateMate input interfacing*

3 Bidirectional Interfacing

In applications in which a GateMate FPGA is connected bidirectionally to peripheral devices, two cases must be distinguished:

1. There is a direction signal available to determine the direction. If it is a bus, all signals always have the same direction.
2. No direction signal is available or it is a bus where the individual signals can have different directions.

3.1 Bidirectional interfacing with direction signal

If a direction signal is available, a circuit with an active bidirectional buffer is recommended. The solution shown in Figure 4 has a delay of less than 10 ns and is therefore also suitable for high speed communication. The 74LV245 or 74LVC245 are 5 V tolerant devices that can be used with 2.5 V supply voltage and are able to have an input voltage of up to 5 V.

> **Please note!**
>
> Please make sure that you use an overvoltage-tolerant device, as the characteristics of the devices from various chip manufacturers may differ.

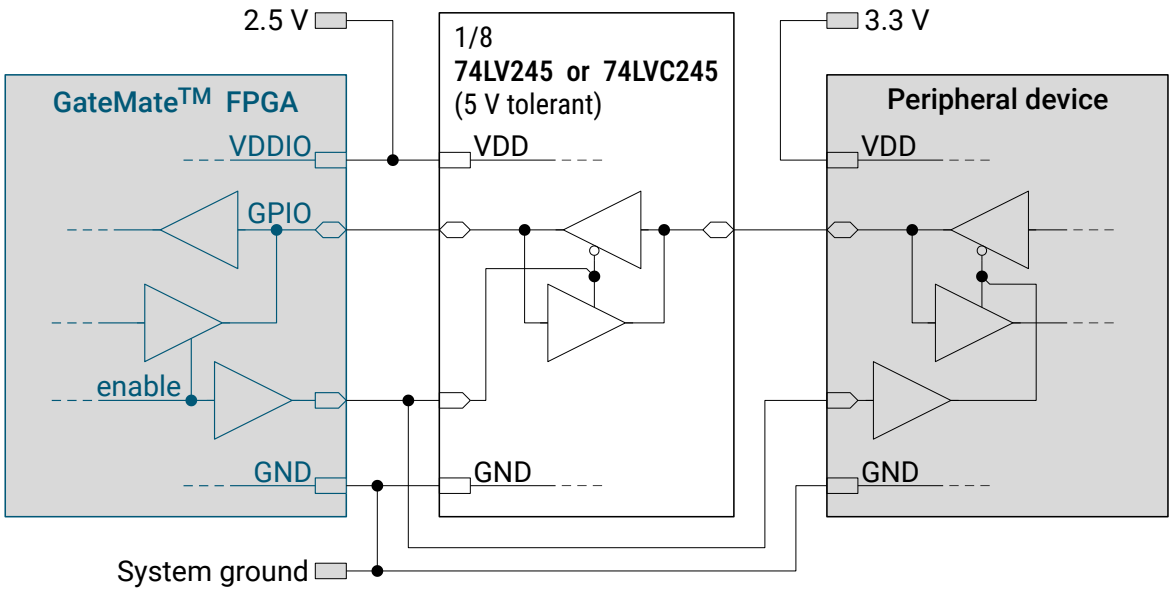

Figure 4: *Bidirectional high speed GateMate interfacing with direction signal*

3.2 Bidirectional interfacing without direction signal

In cases where no direction signal is available, there are devices which can limit the input voltage at both sides. The 8-bit FET bus switch device 74CB3T3245 has a low R_{on} resistance between the two terminals of the FET. This has a delay of less than 6 ns and is therefore also suitable for high speed communications. The 74CB3T3245 device must be used with a supply voltage of 2.5 V to limit the GateMate input voltage to 2.5 V as shown in Figure 5.

This proposed solution has good technical properties, but has higher component costs compared to the bus driver described in the previous section.

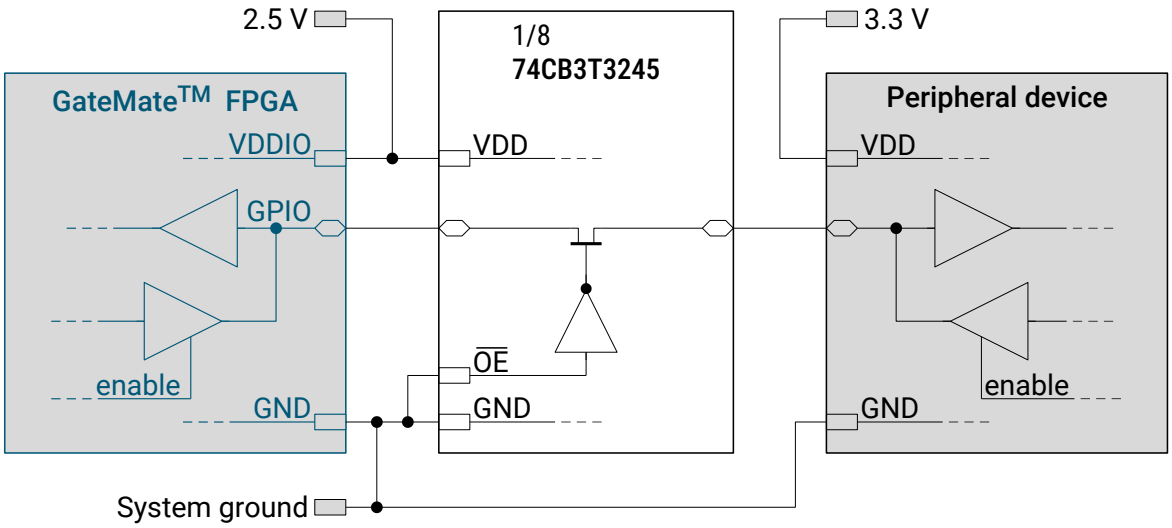

Figure 5: *Bidirectional high speed GateMate interfacing without direction signal*

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