GateMate™ FPGA User Guide

GPIO Bank Allocation of CCGM1A2

UG1004

User Guide June 2025

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About this Document

This User Guide covers the GPIO bank allocation of the CCGM1A2 FPGA from Cologne Chip and is part of the GateMate™ documentation collection.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA
- **DS1001** – GateMate™ FPGA CCGM1A2 Datasheet
- **DS1002** – GateMate™ FPGA Programmer Board Datasheet
- **DS1003** – GateMate™ FPGA Evaluation Board Datasheet
- **UG1001** – GateMate™ FPGA Primitives Library
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide
- **UG1003** – GateMate™ FPGA Interface Guide for Peripheral Devices with 3.3 V Signaling

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1 Introduction

The CCGM1A2 contains two dies of the CCGM1A1, which are interconnected by so-called *die-to-die connections* directly on the silicon. CCGM1A1 and CCGM1A2 are pin compatible, which is why the same design can be used for both FPGAs if the PCB circuitry is designed accordingly.

As CCGM1A2 has twice as many GPIO banks internally as CCGM1A1, not all internal GPIO banks of CCGM1A2 can be routed out to external BGA pins.

The design flow automatically takes this into account. Nevertheless, it is useful for the user to know which internal GPIO banks are available for the circuit design. In addition, there are GPIO banks that are interconnected within the CCGM1A2, increasing the number of usable GPIO banks.

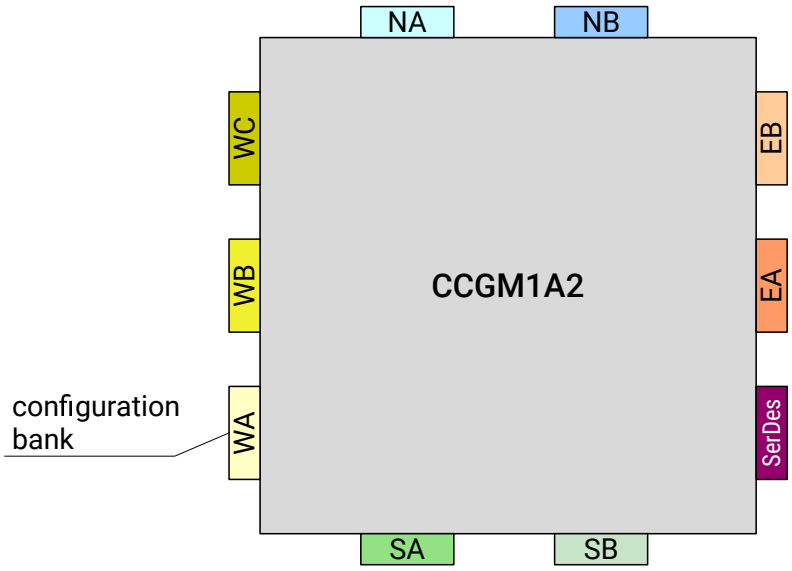

Figure 1: *Overview of CCGM1A2 GPIO banks (chip view)*

2 GPIO Bank Allocation

There are two GPIO banks on each edge of the single-die chip CCGM1A1 named after the cardinal directions north (N), west (W), east (E) and south (S). As an exception, a third bank for configuration signals is attached to the west edge. This basic principle is of course also present in the multi-die chip CCGM1A2 to ensure pin compatibility.

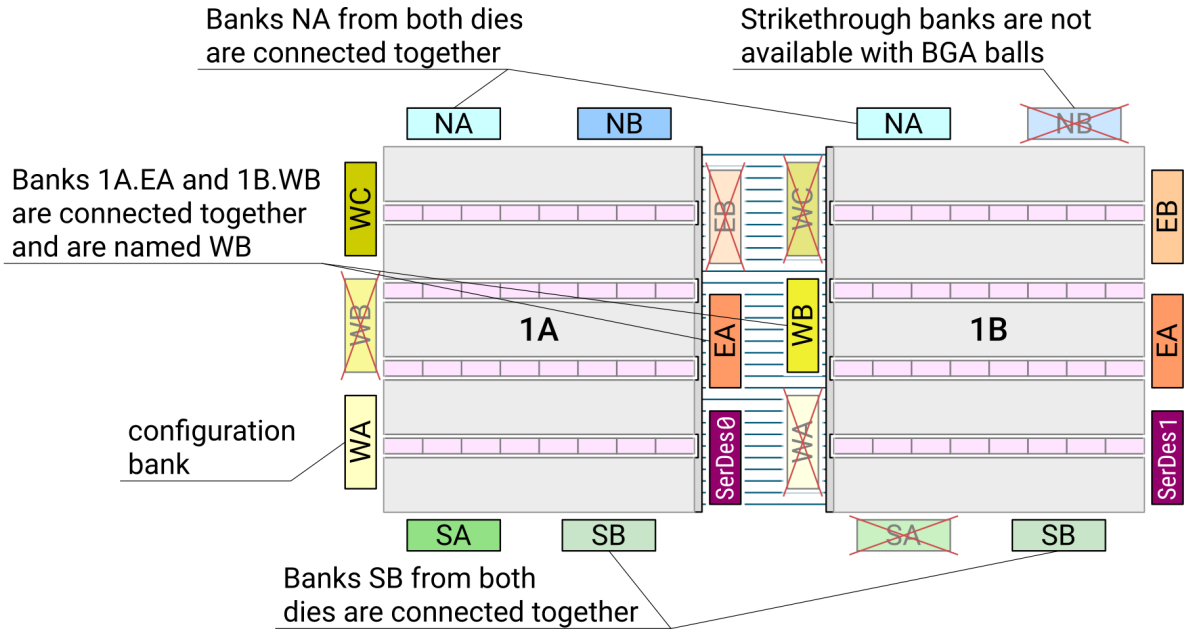

Figure 2: *GPIO banks of CCGM1A2 (chip view)*

Figure 2 shows in detail which internal GPIO banks are routed out. Banks that cannot be used are crossed out.

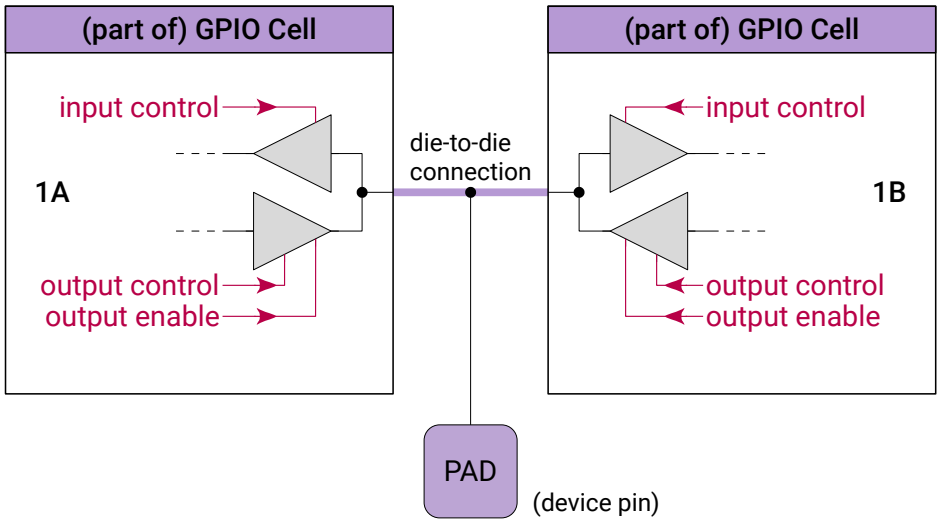

Figure 3: *Interconnection of two GPIO cells from FPGA dies 1A and 1B*

Table 1: *GPIO bank allocation of CCGM1A2*

BGA bank	from die 1A	from die 1B
IO_SA_[A|B][8:0]	SA	
IO_SB_[A|B][8:0]	SB	SB
IO_WA_[A|B][8:0]	WA	
IO_WB_[A|B][8:0]	EA	WB
IO_WC_[A|B][8:0]	WC	
IO_NA_[A|B][8:0]	NA	NA
IO_NB_[A|B][8:0]	NB	
IO_EA_[A|B][8:0]		EB
IO_EB_[A|B][8:0]		EB

As shown in Figure 2, three pairs of GPIO banks are connected internally and are routed out together like shown in Figure 3. This increases the number of available GPIOs.

Each chip can activate the individual ports of these GPIO banks independently of each other, but of course only one of the connected ports can be an output driver.

The interconnection of GPIO banks SB from both FPGA dies connect

$$\begin{aligned} &\texttt{1A.IO\_SB\_A0} - \texttt{1B.IO\_SB\_A0} \\ &\texttt{1A.IO\_SB\_A1} - \texttt{1B.IO\_SB\_A1} \\ &\dots \\ &\texttt{1A.IO\_SB\_A8} - \texttt{1B.IO\_SB\_A8} \end{aligned}$$

in pairs and in the same way

$$\begin{aligned} &\texttt{1A.IO\_SB\_B0} - \texttt{1B.IO\_SB\_B0} \\ &\texttt{1A.IO\_SB\_B1} - \texttt{1B.IO\_SB\_B1} \\ &\dots \\ &\texttt{1A.IO\_SB\_B8} - \texttt{1B.IO\_SB\_B8} \end{aligned}$$

Both banks NA are interconnected in the same way. Finally, with 1A.EA and 1B.WB, two different banks of the FPGA dies are connected to each other.

If the configuration bank WA is omitted from the count because it is only needed once for both FPGA dies, then 11 of the remaining 16 banks are available as shown in Table 1.

3 CCGM1A2 Pinout

Figure 4 shows the pinout of the CCGM1A2 FPGA. Some pins have a second function as shown in Figures 5 and 6.

In both cases, one pin function is GPIO, and according to Figure 5, the configuration bank can alternatively be used as GPIO bank WA, and according to Figure 6, some GPIO pins can be used as dedicated clock inputs.

All ball signals are grouped and color-coded as shown in Table 2.

Besides the 9 GPIO banks there are pin groups for the SerDes interface, power supply,

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	VDD_WC	IO_NA_A0	IO_NA_A1	VDD_NA	IO_NA_A4	GND	IO_NA_A7	IO_NB_B0	GND	IO_NB_B2	IO_NB_B4	GND	IO_NB_B7	IO_EB_B8	VDD_EB	IO_EB_B5	GND	A
B	IO_WC_A8	IO_WC_B8	IO_NA_B0	IO_NA_B1	IO_NA_A2	IO_NA_B4	VDD_NA	IO_NA_B7	IO_NB_A0	VDD_NB	IO_NB_A2	IO_NB_A4	VDD_NB	IO_NB_A7	IO_EB_A8	GND	IO_EB_A5	VDD_EB	B
C	GND	VDD_WC	IO_WC_A7	IO_WC_B7	IO_NA_B2	IO_NA_A3	IO_NA_A5	IO_NA_A6	IO_NA_A8	IO_NB_B1	IO_NB_B3	IO_NB_B5	IO_NB_B6	IO_NB_B8	IO_EB_B7	IO_EB_B6	IO_EB_B4	IO_EB_A4	C
D	IO_WC_A5	IO_WC_B5	IO_WC_A6	IO_WC_B6	VDD_WC	IO_NA_B3	IO_NA_B5	IO_NA_B6	IO_NA_B8	IO_NB_A1	IO_NB_A3	IO_NB_A5	IO_NB_A6	IO_NB_A8	IO_EB_A7	IO_EB_A6	IO_EB_B2	IO_EB_A2	D
E	IO_WC_A3	IO_WC_B3	IO_WC_A4	IO_WC_B4	GND	VDD_NA	GND	VDD_NA	GND	VDD_NB	GND	VDD_NB	GND	VDD_EB	IO_EB_B3	IO_EB_A3	VDD_EB	GND	E
F	GND	VDD_WC	IO_WC_A2	IO_WC_B2	VDD_WC	GND	VDD_NA	GND	VDD	GND	VDD_NB	GND	VDD_EB	GND	IO_EB_B1	IO_EB_A1	IO_EB_B0	IO_EB_A0	F
G	IO_WC_A0	IO_WC_B0	IO_WC_A1	IO_WC_B1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B8	IO_EA_A8	IO_EA_B7	IO_EA_A7	G
H	IO_WB_A7	IO_WB_B7	IO_WB_A8	IO_WB_B8	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B6	IO_EA_A6	VDD_EA	GND	H
J	GND	VDD_WB	IO_WB_A6	IO_WB_B6	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B5	IO_EA_A5	IO_EA_B4	IO_EA_A4	J
K	IO_WB_A5	IO_WB_B5	IO_WB_A4	IO_WB_B4	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B3	IO_EA_A3	IO_EA_B2	IO_EA_A2	K
L	IO_WB_A3	IO_WB_B3	IO_WB_A2	IO_WB_B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B1	IO_EA_A1	VDD_EA	GND	L
M	GND	VDD_WB	IO_WB_A1	IO_WB_B1	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_EA_B0	IO_EA_A0	GND	IO_SB_A3	IO_SB_B3	M
N	IO_WB_A0	IO_WB_B0	SPI_CS_N	SPI_CLK	VDD_WA	VDD	GND	VDD	GND	VDD	VDD_SB	GND	VDD_SB	IO_SB_A8	IO_SB_B8	N.C.	GND	VDD_SB	N
P	SPI_D1	SPI_D0	VDD_WA	GND	VDD_WA	VDD_SA	GND	VDD_SA	GND	VDD_SA	IO_SB_A4	IO_SB_A7	IO_SB_B7	IO_SB_A6	IO_SB_B6	VDD_PLL	IO_SB_A2	IO_SB_B2	P
R	SPI_D3	SPI_D2	JTAG_TCK	SPI_FWD	CFG_MD0	IO_SA_A1	IO_SA_A2	IO_SA_A4	IO_SA_A6	IO_SA_A7	IO_SB_B4	GND	IO_SB_A5	IO_SB_B5	VDD_SB	GND	IO_SB_A1	IO_SB_B1	R
T	VDD_WA	JTAG_TDI	JTAG_TMS	GND	CFG_MD1	IO_SA_B1	IO_SA_B2	IO_SA_B4	IO_SA_B6	IO_SA_B7	GND	SER_CLK	SER_CLK_N	VDD_CLK	RST_N	VDD_SER_PLL	GND	VDD_SB	T
U	POR_EN	JTAG_TDO	VDD_WA	CFG_MD2	IO_SA_A0	VDD_SA	IO_SA_A3	IO_SA_A5	VDD_SA	IO_SA_A8	SER_RX_P0	VDD_SER	SER_TX_P0	SER_RX_P1	GND	SER_TX_P1	IO_SB_A0	IO_SB_B0	U
V	GND	CFG_FAILED_N	CFG_DONE	CFG_MD3	IO_SA_B0	GND	IO_SA_B3	IO_SA_B5	GND	IO_SA_B8	SER_RX_N0	SER_RTERM0	SER_TX_N0	SER_RX_N1	SER_RTERM1	SER_TX_N1	VDD_SER	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 4: *CCGM1A2 FBGA pinout*

ground and a few pins in the gray marked group for other signals.

The pin list is also available for download in csv[1] file format.

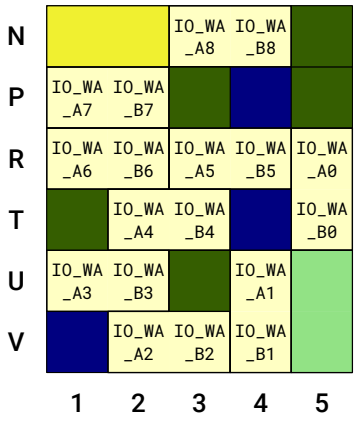

Figure 5: *Configuration pins of CCGM1A2 pinout for use as GPIO after configuration*

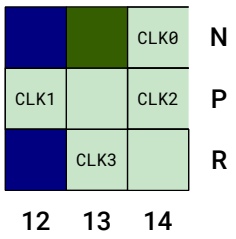

Figure 6: *Clock input pins as second function of some GPIOs*

Table 2: *Pin types*

Color	Pin type	Number of pins
	North general purpose input / output (GPIO) banks NA and NB Each bank has 18 GPIO signals and both have separate power supply balls and can be driven individually. GPIO signals are grouped by pairs and each pair can get configured to be either two single ended or a differential pair signal.	36
	East GPIO banks EA and EB Each bank has 18 GPIO signals and both have separate power supply balls and can be driven individually. GPIO signals are grouped by pairs and each pair can get configured to be either two single ended or a differential pair signal.	36
	South GPIO banks SA and SB Each bank has 18 GPIO signals and both have separate power supply balls and can be driven individually. GPIO signals are grouped by pairs and each pair can get configured to be either two single ended or a differential pair signal.	36

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[1] csv: comma-separated values

Table 2: *Pin types*

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Color	Pin type	Number of pins
	Configuration pins or west GPIO bank WA alternatively The configuration interface consists of 18 pins. After configuration procedure, these balls can be configured to be normal GPIO signals. They are grouped by pairs and each pair can get configured to be either two single ended or a differential pair signal.	18
	West GPIO banks WB and WC Each bank has 18 GPIO signals and both have separate power supply balls and can be driven individually. GPIO signals are grouped by pairs and each pair can get configured to be either two single ended or a differential pair signal.	36
	serializer / deserializer (SerDes) signal pins The SerDes interface consits of differential transmit and receive signals and a termination input pin. Furthermore, dedicated power supply exists to the SerDes interface and the SerDes phase-locked loop (PLL) function.	10
	Power supply pins for FPGA core and GPIO The CCGM1A2 core gets supplied from a single power source. The GPIO banks have own power supply pins each. Additionally, some further power supply pins are available for SerDes and other functions.	78
	Ground pins CCGM1A2 has a single ground level for all supply voltages. All ground pins must be connected.	70
	Any other pins Clock input (single ended or differential), reset input and one not connected pin (must be left open) are available in this pin group.	4

Table 3: *Pin list sorted by ball name*

Ball	Signal name	Signal group	Reset category	Description
A1	GND	Ground	0	Ground
A2	VDD_WC	Power	0	3rd GPIO west bank power supply
A3	IO_NA_A0	GPIO	1	1st GPIO north bank signal A0
A4	IO_NA_A1	GPIO	1	1st GPIO north bank signal A1
A5	VDD_NA	Power	0	1st GPIO north bank power supply
A6	IO_NA_A4	GPIO	1	1st GPIO north bank signal A4
A7	GND	Ground	0	Ground
A8	IO_NA_A7	GPIO	1	1st GPIO north bank signal A7
A9	IO_NB_B0	GPIO	1	2nd GPIO north bank signal B0
A10	GND	Ground	0	Ground
A11	IO_NB_B2	GPIO	1	2nd GPIO north bank signal B2
A12	IO_NB_B4	GPIO	1	2nd GPIO north bank signal B4
A13	GND	Ground	0	Ground
A14	IO_NB_B7	GPIO	1	2nd GPIO north bank signal B7
A15	IO_EB_B8	GPIO	1	2nd GPIO east bank signal B8
A16	VDD_EB	Power	0	2nd GPIO east bank power supply
A17	IO_EB_B5	GPIO	1	2nd GPIO east bank signal B5
A18	GND	Ground	0	Ground
B1	IO_WC_A8	GPIO	1	3rd GPIO west bank signal A8
B2	IO_WC_B8	GPIO	1	3rd GPIO west bank signal B8
B3	IO_NA_B0	GPIO	1	1st GPIO north bank signal B0
B4	IO_NA_B1	GPIO	1	1st GPIO north bank signal B1
B5	IO_NA_A2	GPIO	1	1st GPIO north bank signal A2
B6	IO_NA_B4	GPIO	1	1st GPIO north bank signal B4
B7	VDD_NA	Power	0	1st GPIO north bank power supply
B8	IO_NA_B7	GPIO	1	1st GPIO north bank signal B7
B9	IO_NB_A0	GPIO	1	2nd GPIO north bank signal A0
B10	VDD_NB	Power	0	2nd GPIO north bank power supply
B11	IO_NB_A2	GPIO	1	2nd GPIO north bank signal A2
B12	IO_NB_A4	GPIO	1	2nd GPIO north bank signal A4
B13	VDD_NB	Power	0	2nd GPIO north bank power supply
B14	IO_NB_A7	GPIO	1	2nd GPIO north bank signal A7
B15	IO_EB_A8	GPIO	1	2nd GPIO east bank signal A8
B16	GND	Ground	0	Ground
B17	IO_EB_A5	GPIO	1	2nd GPIO east bank signal A5

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Table 3: *Pin list sorted by ball name*

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Ball	Signal name	Signal group	Reset category	Description
B18	VDD_EB	Power	0	2nd GPIO east bank power supply
C1	GND	Ground	0	Ground
C2	VDD_WC	Power	0	3rd GPIO west bank power supply
C3	IO_WC_A7	GPIO	1	3rd GPIO west bank signal A7
C4	IO_WC_B7	GPIO	1	3rd GPIO west bank signal B7
C5	IO_NA_B2	GPIO	1	1st GPIO north bank signal B2
C6	IO_NA_A3	GPIO	1	1st GPIO north bank signal A3
C7	IO_NA_A5	GPIO	1	1st GPIO north bank signal A5
C8	IO_NA_A6	GPIO	1	1st GPIO north bank signal A6
C9	IO_NA_A8	GPIO	1	1st GPIO north bank signal A8
C10	IO_NB_B1	GPIO	1	2nd GPIO north bank signal B1
C11	IO_NB_B3	GPIO	1	2nd GPIO north bank signal B3
C12	IO_NB_B5	GPIO	1	2nd GPIO north bank signal B5
C13	IO_NB_B6	GPIO	1	2nd GPIO north bank signal B6
C14	IO_NB_B8	GPIO	1	2nd GPIO north bank signal B8
C15	IO_EB_B7	GPIO	1	2nd GPIO east bank signal B7
C16	IO_EB_B6	GPIO	1	2nd GPIO east bank signal B6
C17	IO_EB_B4	GPIO	1	2nd GPIO east bank signal B4
C18	IO_EB_A4	GPIO	1	2nd GPIO east bank signal A4
D1	IO_WC_A5	GPIO	1	3rd GPIO west bank signal A5
D2	IO_WC_B5	GPIO	1	3rd GPIO west bank signal B5
D3	IO_WC_A6	GPIO	1	3rd GPIO west bank signal A6
D4	IO_WC_B6	GPIO	1	3rd GPIO west bank signal B6
D5	VDD_WC	Power	0	3rd GPIO west bank power supply
D6	IO_NA_B3	GPIO	1	1st GPIO north bank signal B3
D7	IO_NA_B5	GPIO	1	1st GPIO north bank signal B5
D8	IO_NA_B6	GPIO	1	1st GPIO north bank signal B6
D9	IO_NA_B8	GPIO	1	1st GPIO north bank signal B8
D10	IO_NB_A1	GPIO	1	2nd GPIO north bank signal A1
D11	IO_NB_A3	GPIO	1	2nd GPIO north bank signal A3
D12	IO_NB_A5	GPIO	1	2nd GPIO north bank signal A5
D13	IO_NB_A6	GPIO	1	2nd GPIO north bank signal A6
D14	IO_NB_A8	GPIO	1	2nd GPIO north bank signal A8
D15	IO_EB_A7	GPIO	1	2nd GPIO east bank signal A7
D16	IO_EB_A6	GPIO	1	2nd GPIO east bank signal A6

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Table 3: *Pin list sorted by ball name*

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Ball	Signal name	Signal group	Reset category	Description
D17	IO_EB_B2	GPIO	1	2nd GPIO east bank signal B2
D18	IO_EB_A2	GPIO	1	2nd GPIO east bank signal A2
E1	IO_WC_A3	GPIO	1	3rd GPIO west bank signal A3
E2	IO_WC_B3	GPIO	1	3rd GPIO west bank signal B3
E3	IO_WC_A4	GPIO	1	3rd GPIO west bank signal A4
E4	IO_WC_B4	GPIO	1	3rd GPIO west bank signal B4
E5	GND	Ground	0	Ground
E6	VDD_NA	Power	0	1st GPIO north bank power supply
E7	GND	Ground	0	Ground
E8	VDD_NA	Power	0	1st GPIO north bank power supply
E9	GND	Ground	0	Ground
E10	VDD_NB	Power	0	2nd GPIO north bank power supply
E11	GND	Ground	0	Ground
E12	VDD_NB	Power	0	2nd GPIO north bank power supply
E13	GND	Ground	0	Ground
E14	VDD_EB	Power	0	2nd GPIO east bank power supply
E15	IO_EB_B3	GPIO	1	2nd GPIO east bank signal B3
E16	IO_EB_A3	GPIO	1	2nd GPIO east bank signal A3
E17	VDD_EB	Power	0	2nd GPIO east bank power supply
E18	GND	Ground	0	Ground
F1	GND	Ground	0	Ground
F2	VDD_WC	Power	0	3rd GPIO west bank power supply
F3	IO_WC_A2	GPIO	1	3rd GPIO west bank signal A2
F4	IO_WC_B2	GPIO	1	3rd GPIO west bank signal B2
F5	VDD_WC	Power	0	3rd GPIO west bank power supply
F6	GND	Ground	0	Ground
F7	VDD_NA	Power	0	1st GPIO north bank power supply
F8	GND	Ground	0	Ground
F9	VDD	Power	0	Core power supply
F10	GND	Ground	0	Ground
F11	VDD_NB	Power	0	2nd GPIO north bank power supply
F12	GND	Ground	0	Ground
F13	VDD_EB	Power	0	2nd GPIO east bank power supply
F14	GND	Ground	0	Ground
F15	IO_EB_B1	GPIO	1	2nd GPIO east bank signal B1

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Table 3: *Pin list sorted by ball name*

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Ball	Signal name	Signal group	Reset category	Description
F16	IO_EB_A1	GPIO	1	2nd GPIO east bank signal A1
F17	IO_EB_B0	GPIO	1	2nd GPIO east bank signal B0
F18	IO_EB_A0	GPIO	1	2nd GPIO east bank signal A0
G1	IO_WC_A0	GPIO	1	3rd GPIO west bank signal A0
G2	IO_WC_B0	GPIO	1	3rd GPIO west bank signal B0
G3	IO_WC_A1	GPIO	1	3rd GPIO west bank signal A1
G4	IO_WC_B1	GPIO	1	3rd GPIO west bank signal B1
G5	GND	Ground	0	Ground
G6	VDD	Power	0	Core power supply
G7	GND	Ground	0	Ground
G8	VDD	Power	0	Core power supply
G9	GND	Ground	0	Ground
G10	VDD	Power	0	Core power supply
G11	GND	Ground	0	Ground
G12	VDD	Power	0	Core power supply
G13	GND	Ground	0	Ground
G14	VDD_EA	Power	0	1st GPIO east bank power supply
G15	IO_EA_B8	GPIO	1	1st GPIO east bank signal B8
G16	IO_EA_A8	GPIO	1	1st GPIO east bank signal A8
G17	IO_EA_B7	GPIO	1	1st GPIO east bank signal B7
G18	IO_EA_A7	GPIO	1	1st GPIO east bank signal A7
H1	IO_WB_A7	GPIO	1	2nd GPIO west bank signal A7
H2	IO_WB_B7	GPIO	1	2nd GPIO west bank signal B7
H3	IO_WB_A8	GPIO	1	2nd GPIO west bank signal A8
H4	IO_WB_B8	GPIO	1	2nd GPIO west bank signal B8
H5	VDD_WB	Power	0	2nd GPIO west bank power supply
H6	GND	Ground	0	Ground
H7	VDD	Power	0	Core power supply
H8	GND	Ground	0	Ground
H9	VDD	Power	0	Core power supply
H10	GND	Ground	0	Ground
H11	VDD	Power	0	Core power supply
H12	GND	Ground	0	Ground
H13	VDD	Power	0	Core power supply
H14	GND	Ground	0	Ground

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Table 3: *Pin list sorted by ball name*

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Ball	Signal name	Signal group	Reset category	Description
H15	IO_EA_B6	GPIO	1	1st GPIO east bank signal B6
H16	IO_EA_A6	GPIO	1	1st GPIO east bank signal A6
H17	VDD_EA	Power	0	1st GPIO east bank power supply
H18	GND	Ground	0	Ground
J1	GND	Ground	0	Ground
J2	VDD_WB	Power	0	2nd GPIO west bank power supply
J3	IO_WB_A6	GPIO	1	2nd GPIO west bank signal A6
J4	IO_WB_B6	GPIO	1	2nd GPIO west bank signal B6
J5	GND	Ground	0	Ground
J6	VDD	Power	0	Core power supply
J7	GND	Ground	0	Ground
J8	VDD	Power	0	Core power supply
J9	GND	Ground	0	Ground
J10	VDD	Power	0	Core power supply
J11	GND	Ground	0	Ground
J12	VDD	Power	0	Core power supply
J13	GND	Ground	0	Ground
J14	VDD_EA	Power	0	1st GPIO east bank power supply
J15	IO_EA_B5	GPIO	1	1st GPIO east bank signal B5
J16	IO_EA_A5	GPIO	1	1st GPIO east bank signal A5
J17	IO_EA_B4	GPIO	1	1st GPIO east bank signal B4
J18	IO_EA_A4	GPIO	1	1st GPIO east bank signal A4
K1	IO_WB_A5	GPIO	1	2nd GPIO west bank signal A5
K2	IO_WB_B5	GPIO	1	2nd GPIO west bank signal B5
K3	IO_WB_A4	GPIO	1	2nd GPIO west bank signal A4
K4	IO_WB_B4	GPIO	1	2nd GPIO west bank signal B4
K5	VDD_WB	Power	0	2nd GPIO west bank power supply
K6	GND	Ground	0	Ground
K7	VDD	Power	0	Core power supply
K8	GND	Ground	0	Ground
K9	VDD	Power	0	Core power supply
K10	GND	Ground	0	Ground
K11	VDD	Power	0	Core power supply
K12	GND	Ground	0	Ground
K13	VDD	Power	0	Core power supply

(continued on next page)

Table 3: *Pin list sorted by ball name*

(continued from previous page)

Ball	Signal name	Signal group	Reset category	Description
K14	GND	Ground	0	Ground
K15	IO_EA_B3	GPIO	1	1st GPIO east bank signal B3
K16	IO_EA_A3	GPIO	1	1st GPIO east bank signal A3
K17	IO_EA_B2	GPIO	1	1st GPIO east bank signal B2
K18	IO_EA_A2	GPIO	1	1st GPIO east bank signal A2
L1	IO_WB_A3	GPIO	1	2nd GPIO west bank signal A3
L2	IO_WB_B3	GPIO	1	2nd GPIO west bank signal B3
L3	IO_WB_A2	GPIO	1	2nd GPIO west bank signal A2
L4	IO_WB_B2	GPIO	1	2nd GPIO west bank signal B2
L5	GND	Ground	0	Ground
L6	VDD	Power	0	Core power supply
L7	GND	Ground	0	Ground
L8	VDD	Power	0	Core power supply
L9	GND	Ground	0	Ground
L10	VDD	Power	0	Core power supply
L11	GND	Ground	0	Ground
L12	VDD	Power	0	Core power supply
L13	GND	Ground	0	Ground
L14	VDD_EA	Power	0	1st GPIO east bank power supply
L15	IO_EA_B1	GPIO	1	1st GPIO east bank signal B1
L16	IO_EA_A1	GPIO	1	1st GPIO east bank signal A1
L17	VDD_EA	Power	0	1st GPIO east bank power supply
L18	GND	Ground	0	Ground
M1	GND	Ground	0	Ground
M2	VDD_WB	Power	0	2nd GPIO west bank power supply
M3	IO_WB_A1	GPIO	1	2nd GPIO west bank signal A1
M4	IO_WB_B1	GPIO	1	2nd GPIO west bank signal B1
M5	VDD_WB	Power	0	2nd GPIO west bank power supply
M6	GND	Ground	0	Ground
M7	VDD	Power	0	Core power supply
M8	GND	Ground	0	Ground
M9	VDD	Power	0	Core power supply
M10	GND	Ground	0	Ground
M11	VDD	Power	0	Core power supply
M12	GND	Ground	0	Ground

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Table 3: *Pin list sorted by ball name*

(continued from previous page)

Ball	Signal name	Signal group	Reset category	Description
M13	VDD	Power	0	Core power supply
M14	IO_EA_B0	GPIO	1	1st GPIO east bank signal B0
M15	IO_EA_A0	GPIO	1	1st GPIO east bank signal A0
M16	GND	Ground	0	Ground
M17	IO_SB_A3	GPIO	1	2nd GPIO south bank signal A3
M18	IO_SB_B3	GPIO	1	2nd GPIO south bank signal B3
N1	IO_WB_A0	GPIO	1	2nd GPIO west bank signal A0
N2	IO_WB_B0	GPIO	1	2nd GPIO west bank signal B0
N3	SPI_CS_N	GPIO	3	1st function: Configuration SPI chip select
N3	IO_WA_A8	GPIO	1	2nd function: 1st GPIO west bank signal A8
N4	SPI_CLK	GPIO	3	1st function: Configuration SPI clock
N4	IO_WA_B8	GPIO	1	2nd function: 1st GPIO west bank signal B8
N5	VDD_WA	Power	0	1st GPIO west bank power supply
N6	VDD	Power	0	Core power supply
N7	GND	Ground	0	Ground
N8	VDD	Power	0	Core power supply
N9	GND	Ground	0	Ground
N10	VDD	Power	0	Core power supply
N11	VDD_SB	Power	0	2nd GPIO south bank power supply
N12	GND	Ground	0	Ground
N13	VDD_SB	Power	0	2nd GPIO south bank power supply
N14	IO_SB_A8	GPIO	1	1st function: 2nd GPIO south bank signal A8
N14	CLK0	GPIO	1	2nd function: 1st clock input
N15	IO_SB_B8	GPIO	1	2nd GPIO south bank signal B8
N16	N.C.	Other	0	Not connected. This pin must be left open.
N17	GND	Ground	0	Ground
N18	VDD_SB	Power	0	2nd GPIO south bank power supply
P1	SPI_D1	GPIO	4	1st function: Configuration SPI data bit 1
P1	IO_WA_A7	GPIO	1	2nd function: 1st GPIO west bank signal A7
P2	SPI_D0	GPIO	3	1st function: Configuration SPI data bit 0
P2	IO_WA_B7	GPIO	1	2nd function: 1st GPIO west bank signal B7
P3	VDD_WA	Power	0	1st GPIO west bank power supply
P4	GND	Ground	0	Ground

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Table 3: *Pin list sorted by ball name*

(continued from previous page)

Ball	Signal name	Signal group	Reset category	Description
P5	VDD_WA	Power	0	1st GPIO west bank power supply
P6	VDD_SA	Power	0	1st GPIO south bank power supply
P7	GND	Ground	0	Ground
P8	VDD_SA	Power	0	1st GPIO south bank power supply
P9	GND	Ground	0	Ground
P10	VDD_SA	Power	0	1st GPIO south bank power supply
P11	IO_SB_A4	GPIO	1	2nd GPIO south bank signal A4
P12	IO_SB_A7	GPIO	1	1st function: 2nd GPIO south bank signal A7
P12	CLK1	GPIO	1	2nd function: 2nd clock input
P13	IO_SB_B7	GPIO	1	2nd GPIO south bank signal B7
P14	IO_SB_A6	GPIO	1	1st function: 2nd GPIO south bank signal A6
P14	CLK2	GPIO	1	2nd function: 3rd clock input
P15	IO_SB_B6	GPIO	1	2nd GPIO south bank signal B6
P16	VDD_PLL	Power	0	PLL power supply
P17	IO_SB_A2	GPIO	1	2nd GPIO south bank signal A2
P18	IO_SB_B2	GPIO	1	2nd GPIO south bank signal B2
R1	SPI_D3	GPIO	4	1st function: Configuration SPI data bit 3
R1	IO_WA_A6	GPIO	1	2nd function: 1st GPIO west bank signal A6
R2	SPI_D2	GPIO	4	1st function: Configuration SPI data bit 2
R2	IO_WA_B6	GPIO	1	2nd function: 1st GPIO west bank signal B6
R3	JTAG_TCK	GPIO	4	1st function: Configuration JTAG clock
R3	IO_WA_A5	GPIO	1	2nd function: 1st GPIO west bank signal A5
R4	SPI_FWD	GPIO	2	1st function: Configuration SPI data forward
R4	IO_WA_B5	GPIO	1	2nd function: 1st GPIO west bank signal B5
R5	CFG_MD0	GPIO	4	1st function: Configuration mode bit 0
R5	IO_WA_A0	GPIO	1	2nd function: 1st GPIO west bank signal A0
R6	IO_SA_A1	GPIO	1	1st GPIO south bank signal A1
R7	IO_SA_A2	GPIO	1	1st GPIO south bank signal A2
R8	IO_SA_A4	GPIO	1	1st GPIO south bank signal A4
R9	IO_SA_A6	GPIO	1	1st GPIO south bank signal A6
R10	IO_SA_A7	GPIO	1	1st GPIO south bank signal A7
R11	IO_SB_B4	GPIO	1	2nd GPIO south bank signal B4
R12	GND	Ground	0	Ground

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Table 3: *Pin list sorted by ball name*

(continued from previous page)

Ball	Signal name	Signal group	Reset category	Description
R13	IO_SB_A5	GPIO	1	1st function: 2nd GPIO south bank signal A5
R13	CLK3	GPIO	1	2nd function: 4th clock input
R14	IO_SB_B5	GPIO	1	2nd GPIO south bank signal B5
R15	VDD_SB	Power	0	2nd GPIO south bank power supply
R16	GND	Ground	0	Ground
R17	IO_SB_A1	GPIO	1	2nd GPIO south bank signal A1
R18	IO_SB_B1	GPIO	1	2nd GPIO south bank signal B1
T1	VDD_WA	Power	0	1st GPIO west bank power supply
T2	JTAG_TDI	GPIO	4	1st function: JTAG data input
T2	IO_WA_A4	GPIO	1	2nd function: 1st GPIO west bank signal A4
T3	JTAG_TMS	GPIO	4	1st function: JTAG test mode select
T3	IO_WA_B4	GPIO	1	2nd function: 1st GPIO west bank signal B4
T4	GND	Ground	0	Ground
T5	CFG_MD1	GPIO	4	1st function: Configuration mode bit 1
T5	IO_WA_B0	GPIO	1	2nd function: 1st GPIO west bank signal B0
T6	IO_SA_B1	GPIO	1	1st GPIO south bank signal B1
T7	IO_SA_B2	GPIO	1	1st GPIO south bank signal B2
T8	IO_SA_B4	GPIO	1	1st GPIO south bank signal B4
T9	IO_SA_B6	GPIO	1	1st GPIO south bank signal B6
T10	IO_SA_B7	GPIO	1	1st GPIO south bank signal B7
T11	GND	Ground	0	Ground
T12	SER_CLK	Other	4	SerDes clock, positive LVDS signal (or single ended)
T13	SER_CLK_N	Other	1	SerDes clock, negative LVDS signal
T14	VDD_CLK	Power	0	Clock signal power supply
T15	RST_N	Other	4	Reset
T16	VDD_SER_PLL	Power	0	SerDes PLL power supply (1.0 V to 1.1 V ±50 mV)
T17	GND	Ground	0	Ground
T18	VDD_SB	Power	0	2nd GPIO south bank power supply
U1	POR_EN	GPIO	2	1st function: Enable power-on reset
U1	IO_WA_A3	GPIO	1	2nd function: 1st GPIO west bank signal A3
U2	JTAG_TDO	GPIO	2	1st function: JTAG data output

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Table 3: *Pin list sorted by ball name*

(continued from previous page)

Ball	Signal name	Signal group	Reset category	Description
U2	IO_WA_B3	GPIO	1	2nd function: 1st GPIO west bank signal B3
U3	VDD_WA	Power	0	1st GPIO west bank power supply
U4	CFG_MD2	GPIO	4	1st function: Configuration mode bit 2
U4	IO_WA_A1	GPIO	1	2nd function: 1st GPIO west bank signal A1
U5	IO_SA_A0	GPIO	1	1st GPIO south bank signal A0
U6	VDD_SA	Power	0	1st GPIO south bank power supply
U7	IO_SA_A3	GPIO	1	1st GPIO south bank signal A3
U8	IO_SA_A5	GPIO	1	1st GPIO south bank signal A5
U9	VDD_SA	Power	0	1st GPIO south bank power supply
U10	IO_SA_A8	GPIO	1	1st GPIO south bank signal A8
U11	SER_RX_P0	SerDes	1	Receive data line of interface 0, positive LVDS signal
U12	VDD_SER	Power	0	SerDes core power supply (1.0 V to 1.1 V ±50 mV)
U13	SER_TX_P0	SerDes	1	Transmit data line of interface 0, positive LVDS signal
U14	SER_RX_P1	SerDes	1	Receive data line of interface 1, positive LVDS signal
U15	GND	Ground	0	Ground
U16	SER_TX_P1	SerDes	1	Transmit data line of interface 1, positive LVDS signal
U17	IO_SB_A0	GPIO	1	2nd GPIO south bank signal A0
U18	IO_SB_B0	GPIO	1	2nd GPIO south bank signal B0
V1	GND	Ground	0	Ground
V2	CFG_FAILED_N	GPIO	2	1st function: Configuration failed signal
V2	IO_WA_A2	GPIO	1	2nd function: 1st GPIO west bank signal A2
V3	CFG_DONE	GPIO	2	1st function: Configuration done signal
V3	IO_WA_B2	GPIO	1	2nd function: 1st GPIO west bank signal B2
V4	CFG_MD3	GPIO	4	1st function: Configuration mode bit 3
V4	IO_WA_B1	GPIO	1	2nd function: 1st GPIO west bank signal B1
V5	IO_SA_B0	GPIO	1	1st GPIO south bank signal B0
V6	GND	Ground	0	Ground
V7	IO_SA_B3	GPIO	1	1st GPIO south bank signal B3
V8	IO_SA_B5	GPIO	1	1st GPIO south bank signal B5

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Table 3: *Pin list sorted by ball name*

(continued from previous page)

Ball	Signal name	Signal group	Reset category	Description
V9	GND	Ground	0	Ground
V10	IO_SA_B8	GPIO	1	1st GPIO south bank signal B8
V11	SER_RX_N0	SerDes	1	Receive data line of interface 0, negative LVDS signal
V12	SER_RTERM0	SerDes	0	Line termination of interface 0
V13	SER_TX_N0	SerDes	1	Transmit data line of interface 0, negative LVDS signal
V14	SER_RX_N1	SerDes	1	Receive data line of interface 1, negative LVDS signal
V15	SER_RTERM1	SerDes	0	Line termination of interface 1
V16	SER_TX_N1	SerDes	1	Transmit data line of interface 1, negative LVDS signal
V17	VDD_SER	Power	0	SerDes core power supply (1.0 V to 1.1 V ±50 mV)
V18	GND	Ground	0	Ground

Reset categories:

- **0:** No reset (supply or analog input pin)
- **1:** Pin disabled, high-z
- **2:** Pin characteristic already during reset state
- **3:** Pin characteristic depends on the configuration mode (SPI master: I/O, else: input)
- **4:** Input pin

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